Jpn. J. Appl. Phys. Vol. 39 (2000) pp. L 694–L 697
Part 2, No. 7A, 1 July 2000
©2000 The Japan Society of Applied Physics

Single Wafer Furnace and Its Thermal Processing Applications

Woo Sik YOO, Takashi FUKADA, Hiromitsu KURIBAYASHI, Hirofumi KITAYAMA[1],
Nobuaki TAKAHASHI[2], Keiichi ENJOJI[2] and Kiyoshi SUNOHARA[2]

WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112, U.S.A.
[1]*Tokyo Electron Yamanashi Limited, 2381-1 Kitagejo, Fujii-cho, Nirasaki, Yamanashi 407-8511, Japan*
[2]*Tokyo Electron Limited, 3-6 Akasaka 5-chome, Minato-ku, Tokyo 107-8481, Japan*

(Received March 8, 2000; accepted for publication May 19, 2000)

A resistively heated, vacuum and atmospheric pressure compatible, single wafer furnace (SWF) system is proposed to improve operational flexibility of conventional furnaces and productivity of single wafer rapid thermal processing (RTP) systems. The design concept and hardware configuration of the SWF system are described. The temperature measurement/control techniques and thermal characteristics of the SWF system are described. Typical process results in TiSi formation, implant anneal and thin oxide formation using the SWF system are reported. Due to the vertically stacked, dual chamber configuration and steady state temperature control, very flexible operation with a high throughput at a minimal power consumption (<3.5 kW per process chamber at 1150°C) was realized. Many thermal processes used in furnaces and RTP systems can easily be converted to SWF processes without decreasing cost performance and/or deteriorating process results by using the SWF system.

KEYWORDS: single wafer furnace (SWF), rapid thermal processing (RTP), furnace, silicide, oxidation, thermal budget, sheet resistance, uniformity, throughput, power consumption

1. Introduction

Thermal processing applications such as dopant diffusion, annealing, oxidation, nitridation and thermal chemical vapor deposition (CVD) have always been at the center of silicon semiconductor device fabrication processes since its industry's inception. Horizontal batch furnaces were used for a long time, then vertical batch furnaces were introduced to improve temperature uniformity and efficiency of cleanroom space usage. Batch furnaces are able to meet the requirements for many thermal processing applications even for 0.18 μm technology.[1)]

As device dimensions and allowable thermal budgets (more precisely, integral of diffusivity during thermal process) decrease, many thermal processing applications are performed in single wafer rapid thermal processing (RTP) systems. The need for improved ambient control due to the introduction of new materials requires single wafer processing system. Besides the technical reasons, the flexibility in processing lot size, reduced cycle time and the ability for wafer-to-wafer quality control from the risk management point of view provided by single wafer processing make the single wafer processing more attractive.[1–3)] Typical RTP systems employ either halogen lamps or resistively heated susceptor as heat source.[4)] The lamp based RTP systems have very poor energy efficiency and requires complicated temperature measurement/control algorithms. Although the susceptor based RTP systems have higher energy efficiency, they cannot be used in an oxidation environment due to the oxidation of susceptor material.[5)]

To overcome the drawbacks of batch furnaces and single wafer RTP systems, a single wafer furnace (SWF) with a vacuum loadlock is designed. In this paper, the design concept and thermal behavior of a vacuum and atmospheric pressure compatible dual chamber SWF system are described. Wafer temperature characterization results during ramp-up, ramp-down and preliminary process results using the SWF system are described.

2. System Configuration and Process Chamber

The SWF controls process chamber temperature steady state and move wafers in and out of preheated process chamber instead of controlling wafer temperature directly. The SWF process chamber consists of a transparent quartz reactor, a silicon carbide cavity, a heater assembly and an aluminum housing. Two vertically stacked process chambers are attached to one side of the wafer transport module. The stack of a vacuum loadlock and two cooling stations are attached to the other side of the wafer transport module to reduce the footprint of the system. (Fig. 1(a)). The system is vacuum and atmospheric pressure compatible. Since the process chamber is made of quartz, the system can be used in oxidation as well as annealing applications. A cross-section of the SWF pro-

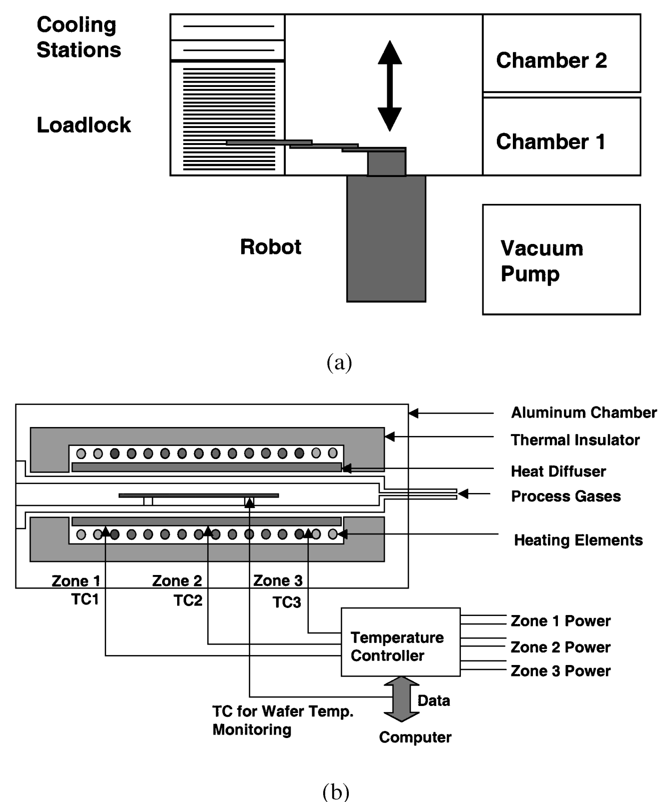

Fig. 1. (a) Single wafer furnace configuration. (b) Schematic illustration of process chamber.

cess chamber is shown in Fig. 1(b). The process chamber has three standoffs made of quartz and no moving parts inside. An R-type (Pt-13% Rh/Pt) thermocouple is embedded in one of the quartz standoffs to monitor idle process environment temperature and wafer temperature during process. The wafer is placed on the quartz standoffs (8–9 mm tall) in the middle of process chamber. The distance between wafer and quartz walls is kept at ~10 mm for both up and downward directions. The quartz process chamber is located in a SiC cavity which acts as heat distributor to create isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly.

The entire unit (quartz process chamber, SiC cavity and heater assembly) is enclosed inside an aluminum chamber. The wafers can be processed in either vacuum or atmospheric pressure (1–760 Torr). In the SWF process chamber, the temperature of the SiC cavity is monitored by three embedded R-type thermocouples and controlled by the three zone heater assembly using feedback signals from the thermocouples to provide identical and nearly isothermal environment to wafers regardless of wafer conditions. The process chamber temperature is kept constant at predetermined temperature. A nearly isothermal environment where the wafer is processed is created by the SiC cavity with very high thermal conductivity.

3. Wafer Temperature Profile during Process

Wafer temperature profile during process at different process chamber (SiC cavity) temperatures is monitored using a thermocouple embedded instrumentation wafer (Fig. 2). The wafer temperature measurement was done under 760 Torr air environment. The idle process environment temperature and wafer temperature during process can also be monitored by the embedded R-type thermocouple in one of the quartz standoffs. Wafer handling sequence is as follows: (1) wafer is introduced into process chamber by wafer handling robot, (2) robot lowers the wafer to standoffs, (3) the robot leaves the process chamber, (4) hold wafer in the process chamber for process time and (5) robot removes wafer from process chamber at process temperature.

As seen in Fig. 2, wafer is heated as soon as it is introduced in the preheated process chamber. Wafer temperature

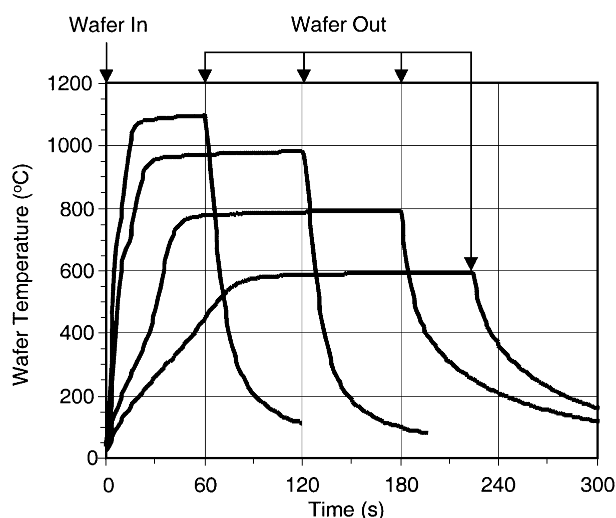

Fig. 2. Wafer temperature profile during process at different temperatures.

increases approximately exponentionally and approaches furnace temperature with time. Initial ramp rate is ranging from ~150°C/s at a furnace temperature of 1100°C. The higher furnace temperature, the higher initial ramp rate. Wafer is quickly removed after processing at almost process temperature and placed into cooling station. An exponential ramp down is observed during natural radiation cool down. Wafer cooling is generally done in cooling station. Wafer temperature reaches 60°C in less than 60 s from wafer retrieval at 1100°C when cooling station is used.

Typical lamp heated RTP systems require wafer rotation to minimize within-wafer temperature non-uniformity due to pattern transfer from lamp array during process. They also require purge, preheating and wafer cooling steps before and after the process. To prevent slip generation during high temperature processes, dynamic zone temperature control and slip prevention hardware such as a Si or SiC ring are employed. Fast ramp-up without temperature overshooting has always been a significant technical challenge for lamp heated RTP system design. Process time referred in lamp heated RTP system is the soak time near process temperature regardless of overhead times such as preheating, ramp-up and ramp-down times.

In a SWF system, temperature overshooting is simply not possible by nature and excellent temperature repeatability is given as long as the SiC cavity temperature remains constant. Process time referred in this paper is the wafer residence time (from wafer-in to wafer-out) in a heated process chamber. The exponential ramp-up and ramp-down is considered to be ideal for a wafer-friendly, efficient thermal processing without increasing unnecessary process steps which result in thermal budget increase and productivity decrease.

4. Process Results and Discussion

The shape effect of heated cavities on within wafer temperature uniformity was investigated using two different types of SiC cavities. One cavity was configured with two SiC parallel plates (284 mm × 270 mm × 5 mm) which was surrounded by a heater assembly. The other cavity was configured with a one piece SiC tube with a rectangular cavity inside. The distance between the SiC planes in both cavities were kept constant at 26 mm. The within wafer temperature uniformity was evaluated in terms of process uniformity as well as crystalline slip generation in the temperature range of 600–1150°C.

At temperatures below 800°C, very uniform process results were obtained regardless of SiC cavity configuration. When two parallel plates are used as a heat diffuser, heat loss from the edge of the parallel plates and the wafer make the within wafer temperature uniformity worse at temperature above 800°C. In the case of a one piece SiC tube cavity, we were able to maintain excellent within wafer temperature uniformity in the temperature range of 600–1150°C by controlling the power of both ends of the SiC cavity. Process uniformity was investigated using the one piece SiC cavity as a heat diffuser.

Figure 3 shows sheet resistance contour maps for 200 mm diameter wafers before and after TiSi formation. The sheet resistance was measured using a four point probe and 5 mm from wafer edge was excluded in measurement. The thickness of Ti films was 80 nm. The annealing condition for TiSi formation was 600°C/60 s and 800°C/60 s. The uniformity

	Rs before anneal	Rs after anneal
600°C 60s	6.976 ohm/sq 1.572%	12.854 ohm/sq 2.150% Unif. Change 0.578%
800°C 60s	6.964 ohm/sq 1.473%	0.953 ohm/sq 1.624% Unif. Change 0.151%

Fig. 3. Sheet resistance contour maps of Ti (before process) and TiSi (after process) layers on 200 mm wafer. (Ti film thickness: 80 nm, pressure: 760 Torr, process time: 60 s, N_2 flow: 1 slm)

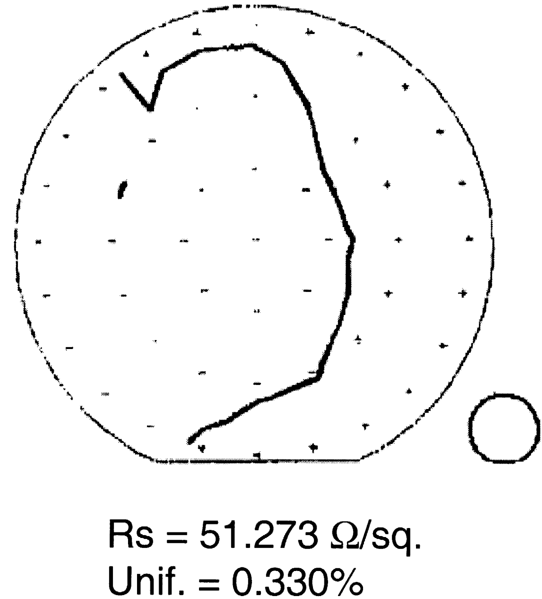

Fig. 4. Sheet resistance contour map of As^+ implant wafer after annealing (dose: $^{75}As^+$ $1 \times 10^{16}/cm^2$, temperature: 915°C, pressure: 760 Torr, process time: 85 s, N_2 flow: 1 slm).

change in 1σ after process of wafers was less than 1.0%, suggesting excellent within-wafer temperature uniformity during the process. Excellent within-wafer temperature uniformity was achieved over the entire silicidation temperature range.

Sheet resistance uniformity of an arsenic implant wafer ($^{75}As^+$ 80 keV, $1 \times 10^{16}/cm^2$) after annealing is shown in Fig. 4. Annealing was done at 915°C for 85 s under 760 Torr N_2. The sheet resistance and uniformity were 51.27 Ω/sq. and 0.33% (1σ), respectively.

Thin oxide films were grown on 200 mm diameter Si wafers. Dry oxidation was done at 1050°C under 100% O_2 760 Torr. Process time was varied from 60 to 3600 s and oxygen flow of 3 slm was maintained throughout the process. Figure 5 shows thickness contour map of thin oxide formed for 120 s in SWF process chamber. Oxide thickness was measured by ellipsometry. An average film thickness of 8.5 nm with uniformity of $\sim$1.0% in 1σ was obtained.

To investigate temperature uniformity and thermal shock during high temperature process ($>$1000°C), bare Si wafers were annealed 1 to 10 times in the temperature range of 800–1150°C. We were able to anneal Si wafers without generating any slip lines in the temperature range of interest. X-ray topography does not indicate any slip generation in wafers processed 5 times repeatedly in the SWF system at 1100°C for 60 s under 760 Torr in air after process parameter optimization. Process optimization details of slip prevention will be published separately.

Process and slip test results obtained using the SWF system are equivalent or better than those obtained from the conventional lamp heated RTP systems. Feasibility of a new RTP system with a very simple design was demonstrated. High thermal conductivity and diffusivity of SiC cavity and optimized geometry of heater zones made this possible. Lamp based RTP systems are limited to applications with relatively shorter processing time due to the hardware limitations such as reliability and lifetime of lamps, and temperature increase of quartz windows and lamp housings. Since the SWF has no hardware limitations affecting the length of process time, many batch furnace processes can also be done in the system

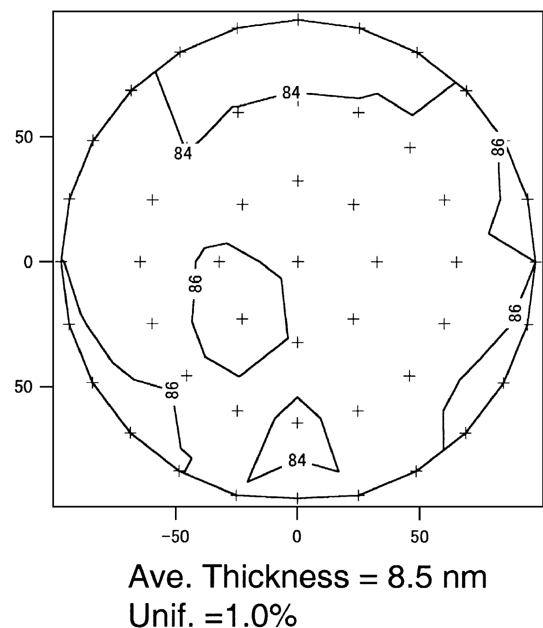

Fig. 5. Thickness contour map of thin oxide film (temperature: 1050°C, pressure: 760 Torr, process time: 120 s, O_2 flow: 3 slm).

with increased process flexibility and short cycle time.

Dual process chamber configuration of the SWF system provides greater flexibility in process temperature while keeping process chamber temperature constant. Many silicide requires two step (formation and annealing) processes at two different temperatures. In the SWF system, each process chamber can be set at different temperature. In other words, one SWF system can handle the first (formation) step and the second (annealing) step without waiting temperature change and stabilization from one temperature to the other. Due to dual process chamber configuration and very efficient temperature ramp up/down characteristics of the SWF system, a very high wafer throughput is achieved. Throughputs of

60–70 wafers per hour can be achieved for 60 s processes with a 60 s cool down step. Average steady state power consumption at 1150°C is <3.5 kW per process chamber. Since the SiC cavity temperature is controlled at steady state, peak power requirement does not normally exceed twice the average steady state power consumption. In contrast, lamp based RTP systems consume a peak power of 50–250 kW per process chamber at a temperature set point of 1000°C depending on the number of lamps and lamp array.

5. Summary

The concept and feasibility of a vacuum and atmospheric pressure compatible, dual chamber SWF system were demonstrated with TiSi, As^+ implant anneal and dry oxidation processes. The temperature measurement/control techniques and thermal characteristics of the SWF system were described and compared with those of conventional lamp heated RTP systems. Uniformity change in sheet resistance before and after process was kept below 1.0% (1σ) in both TiSi process. The As^+ implantation anneal and dry oxidation results also showed an excellent uniformity of 1.0% (1σ) or less. Due to the dual process chamber configuration and steady state temperature control, a very high throughput (60–70 wafers per hour for 60 s process) at a minimal power consumption (<3.5 kW at 1150°C) was achieved. Many furnace processes can easily be converted to SWF processes without decreasing productivity. Thermal budget and process cycle time will be reduced significantly. Most of RTP processes can also be done without decreasing cost performance and/or deteriorating process results by using the SWF system.

Acknowledgements

The authors would like to thank Mr. Y. Hiraga, Mr. D. Carman, Mr. K. Kang, Ms. J. Lau and Mr. T. Yamazaki of WaferMasters, Inc. for useful discussions and encouragement throughout this work.

1) J. K. Truman, C. M. Gronet, N. L. Kuan, C. M. Czarnik, G. E. Miner, D. C. Jennings and I. Beinglass: *Proc. 7th Int. Conf. Advanced Thermal Processing of Semiconductors-RTP'99* (Colorado Springs, 1999) p. 6.
2) C. Ratliff, T. Koble, R. Sloan, S. Sedehi, A. Helms, Jr., J. Kowalski and T. Qiu: *Proc. 7th Int. Conf. Advanced Thermal Processing of Semiconductors-RTP'99* (Colorado Springs, 1999) p. 16.
3) A. L. Helms, Jr., R. B. Herring, C. Porter and A. Starner: Solid State Technol. **42**, No. 11 (1999) 83.
4) F. Roozeboom: *Advances in Rapid Thermal & Integrated Processing*, ed. F. Roozeboom (The Netherlands, 1996) NATO ASI Series E, Vol. 318, Chap. 1.
5) W. S. Yoo, A. J. Atanos and J. F. Daviet: Jpn. J. Appl. Phys. **37** (1998) L1135.