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Design of Single-Wafer Furnace and Its Rapid Thermal Processing Applications

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A resistively heated, vacuum- and atmospheric-pressure-compatible, single-wafer furnace (SWF) system is designed to improve the operational flexibility of conventional furnaces and the productivity of single-wafer rapid thermal processing (RTP) systems. The heat source design and system operation concepts are described. The temperature measurement/control techniques and thermal characteristics of the heat source are described. The heat transfer mechanism between the heat source and Si wafer is discussed. Temperature and process uniformity in SWF were demonstrated in TiSi formation, implant annealing and thin-oxide formation. The defect-generation phenomenon in Si wafers during atmospheric pressure RTP in a SWF system is investigated as a function of temperature, process time, wafer handling method and speed. Highly repeatable slip-free RTP results were achieved in 200-mm-diameter Si wafers processed at 1100°C for 60 s (up to 5 times) through the optimization of the wafer handling method and speed.

KEYWORDS: single-wafer furnace (SWF), rapid thermal processing (RTP), furnace, heat transfer mechanism, defect generation, slip, X-ray topography

1. Introduction

Horizontal batch furnaces have been used in thermal processing applications such as dopant diffusion, annealing, oxidation, nitridation and thermal chemical vapor deposition (CVD) since the inception of semiconductor industry. Vertical batch furnaces were then introduced to improve the temperature uniformity and efficiency of clean room space usage. Both types of batch furnaces are widely used and able to meet the requirements for many thermal processing applications, even for 0.18 μm gate technology.[1)]

As device dimensions and allowable thermal budgets (more precisely, integral of diffusivity during thermal process) decrease, many thermal processing applications are coming to be performed in single-wafer rapid thermal processing (RTP) systems. The need for improved ambient control with the introduction of new materials requires a single-wafer processing system. Single-wafer RTP technology has significant advantages over thermal processing in conventional batch furnaces (150–200 wafers/batch) in terms of thermal budget reduction and process flexibility improvement in temperature range and lot sizes.[1)] Typical furnace process times ranged from 4 to 6 h per batch. A high temperature process time could approach 10 h per batch. Typical ramp-up and ramp-down rates in standard vertical furnaces are ~10°C/min and ~3°C/min, respectively.[2)] Typical process times in the RTP system are 1 to 5 min per wafer while the ramp-up and ramp-down rates range from 20°C/s to 250°C/s. Rapid wafer temperature ramping-up and ramping-down renders the thermal process very efficient without increasing the thermal budget.[3)] A small temperature gradient on wafers heated above 1000°C, however, can cause plastic deformations (crystalline slips) which strongly affect the device yield.[4)] Slip-free RTP of large-diameter (200 mm and larger) Si wafers is still a significant technical challenge.[5)]

Typical cold-wall-type RTP systems employ halogen lamps to heat wafers by optical interaction between light source (lamps) and wafers. The hot-wall-type RTP systems use a resistively heated susceptor as a heat source. Lamp-based RTP systems have very poor energy efficiency and require complicated temperature measurement/control algorithms to maintain within-wafer temperature uniformity during processing and minimize temperature overshooting or undershooting. Although susceptor-based RTP systems have higher energy efficiency, they can only be used in low-pressure (<100 Torr) non-oxidation environments due to the susceptor material (SiC-coated graphite), because of large heat loss from the susceptor to the water-cooled chamber wall through gas conduction as well as radiation.[6)]

We have designed a single-wafer furnace (SWF) with a vacuum load lock to overcome the drawbacks of batch furnaces and single-wafer RTP systems.[7,8)] In this paper, the design concept and thermal behavior of the heat source are described in detail. Theoretical calculation results on heat source configurations are discussed. Wafer temperature characterization results during ramping-up and ramping-down as well as typical process results using the heat source are described. The defect-generation phenomenon in 200-mm-diameter Si wafers during RTP in a SWF and the defect elimination method is discussed. Slip-free RTP process results are obtained by process parameter optimization.

2. Heat Source Design

Designing a uniform heat source is the most important task in achieving repeatable and uniform process results without adjustments. In order to uniformly heat a large-diameter semiconductor wafer, a uniform planar heat source is desired rather than arrays of linear or point heat sources. However, the development of a large-area, planar-heating element is impractical from the view point of balancing physical properties such as electrical resistivity, thermal conductivity, thermal diffusivity, thermal mass, thermal expansion, material uniformity and manufacturability. Prior to designing the heat source, the geometrical effect of a heat source on a wafer is theoretically calculated. Calculation results were reflected in the heat source design.

2.1 Heat transfer mechanism

At low temperatures (<800°C), heat transfer between a heat source and a heated object (Si wafer) is dominated

by conduction and convection. Heat transfer by convection is significant only if the ambient pressure is reasonably high and the heat source is placed at the bottom. As the heat source temperature increases, the radiation heat transfer (exchange) becomes dominant. Since the radiation heat exchange strongly depends on surface conditions (emissivity, reflectivity, roughness etc.), geometries and orientations, the heating element must be appropriately configured to obtain reasonable temperature uniformity at high temperatures (>800°C).

In the case of heating Si wafers, the optical properties of Si must be considered. Lightly doped Si has an absorption edge at approximately 1.2 μm and is semitransparent in the infrared (IR) region. As the temperature of Si increases, Si becomes less transparent and finally becomes opaque at a temperature approximately 600°C in the IR region. The radiation heat exchange between the heat source and the Si wafer becomes very efficient at Si wafer temperatures above 600°C. Highly doped Si wafers are less transparent in the IR region even at low temperatures (<600°C) and easily absorb IR photons. Consequently, highly doped Si wafers will heat up faster under the same heat source condition. The radiation heat exchange becomes very complex when there is variation in dopant concentration, material (i.e., poly-Si, metal and dielectric layers) and structure. Si wafers with device patterning will also behave differently.[9)]

As long as a wafer does not come into contact with a heat source, conduction and convection are the main heat transfer mechanisms at temperatures below 600°C. The wafer temperature uniformity can be easily obtained by using a uniform heat source because the thermal conductivity of Si (1.48 W/mK at room temperature) is more than three orders of magnitude higher than that of ambient gas (for air, 2.62×10^{-2} W/mK at room temperature, 1 atm).[10)] As the heat source temperature and Si wafer temperature increase, the radiation heat exchange becomes the major path. In this case, a view factor (also called a configuration or shape factor) must be considered in addition to the temperature uniformity of heat source in order to understand heat transfer, radiation heat loss and temperature uniformity on a Si wafer. To design a heat source, which provides uniform temperature on a wafer in a wide operating temperature range (200–1200°C), the effect of heating element configuration at high temperatures where radiation exchange is dominant must be investigated.

2.2 *Effect of heating element configuration*

The effect of radiation heat transfer from a linear heating element array was calculated on the observation plane at predetermined distances under the heating elements. The diameter of heating elements, number of heating elements, pitch between heating elements, and distance between the heating elements and the observation plane were varied. For simplicity, the temperature of each heating element is assumed to be the same. The view angle of the heating element array on the plane was calculated. Figures 1(a) and 1(b) show the normalized view angle and absolute view angle on the plane at distance $d = 10$ mm from heating elements with three different diameters (1, 5 and 10 mm). The number of heating elements and pitch were fixed at 11 and 30 mm, respectively. The heating element configuration is illustrated in the inset of Fig. 1(a). Variation in the normalized view angle becomes smaller and the absolute view angle becomes larger as the heating element diameter increases. The heating elements with a larger diameter and/or larger heating element density, increases the heat-source surface area and the view angle from the observation plane. As the surface area increases, the heating element temperature required in order to exchange the same amount of heat by radiation becomes lower. A planar heat source is required for obtaining the least temperature variation in both the heat source and the wafer. The normalized and absolute view angles decrease as the observation point moves away from the center of the heating element array. They also decrease as the distance between the heating elements and the plane increases. This suggests that a finite heat source with uniform temperature cannot provide temperature uniformity on a wafer when the radiation heat transfer becomes dominant.

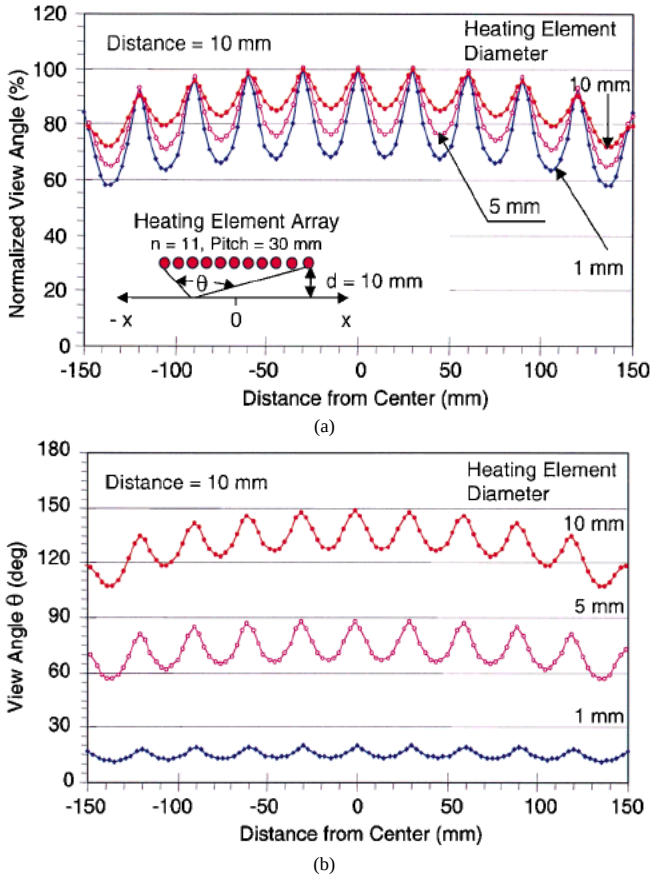

Fig. 1. Normalized view angle (a) and absolute view angle (b) on the plane at distance $d = 10$ mm from heating elements with diameters of 1, 5 and 10 mm (number of heating element = 11, pitch = 30 mm).

The heating element configuration plays a significant role in the temperature uniformity of the heat source as well as that of the wafer. Linear or circular arrays of heating elements are widely used as heat sources in thermal processing equipment such as furnaces and RTP systems. To obtain reasonable temperature uniformity on wafers, multiple zone power control and/or a wafer rotation mechanism are frequently used for heat loss compensation in commercially available systems.

2.3 *Effect of distance between heat source and wafer*

The distance between the heat source and the wafer affects the efficiency of heat transfer through ambient gas as well as radiation. As described in the heat transfer mechanism section, the heat transfer between the heat source and wafer by ambient gas conduction is dominant at low temperatures (<800°C). The radiation heat transfer becomes dominant at high temperatures (>800°C). At a given heat source size, a small distance between the heat source and wafer results in better heat transfer through ambient gas. The view factor is also a very strong function of the distance and angle between the heat source and wafer. To estimate the geometrical effect of radiation heat transfer, the view factor for coaxial parallel disks was calculated as a function of disk size and distance between disks. The diameter of one disk is fixed at a Si wafer size of 200 mm while the diameter of the other disk (heat source) is varied from 200 mm to 400 mm. The distance d between the disks was varied from 5 mm to 300 mm. As shown in Fig. 2, the view factor decreases as the heat source diameter decreases and the distance increases. When the distance is sufficiently small (<10 mm), the view factor between coaxial parallel disks is almost 1.0 and less dependent on the diameter of heat source. A larger uniform heat source provides better temperature uniformity on the wafer, but the size of the heat source must be practical. A heat source diameter of 300 mm provides design flexibility as well as sufficient radiation heat exchange considering the calculated view factor values.

2.4 *Edge effect in radiation heat transfer*

When a wafer is placed under a heat source with a limited size, the view angle from the wafer center to the heat source differs from that from the wafer edge. If the difference in view angle between the wafer center and the edge is large, temperature uniformity on the wafer will be poor even though the temperature uniformity on the heat source is excellent. Figure 3 shows the calculated view angle as a function of distance from the center of the heat source with respect to the observation plane, which is parallel to the heat source plane. The size of the heat source is fixed at 300 mm for the view angle calculation. For simplicity, a two-dimensional model was used in the calculation. The distance between the heat source plane and the observation plane is varied from 10 mm to 200 mm. As shown in Fig. 3, the change in view angle is gradual when the distance between the heat source plane and the observation plane is large. With keeping the distance small, an abrupt change in the view angle is observed near the edge of heat source. In the case of $d = 10$ mm, the view angle at the 200-mm-diameter wafer edge (100 mm from center) is only 3.5% smaller than that at the center. It is important to keep the distance between the heat source and the wafer small to improve radiation heat transfer efficiency as well as to minimize the view angle variation on the wafer. The authors believe that a ~300-mm-diameter heat source and a distance of ~10 mm between the heat source and the wafer are appropriate for heating a 200-mm-diameter Si wafer with reasonable temperature uniformity.

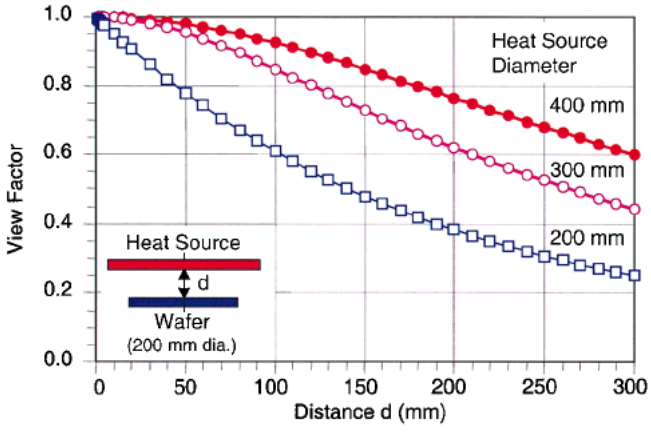

Fig. 2. View factor calculation results for coaxial parallel disks as a function of disk size and distance between disks.

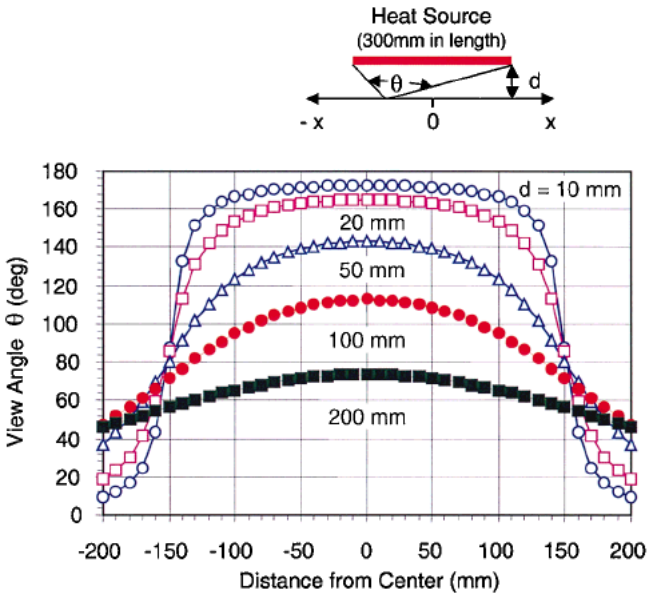

Fig. 3. Spatial distribution of view angle with respect to 300-mm-diameter heat source from observation plane.

2.5 *Effect of heat diffuser*

To fabricate a uniform planar heat source using discrete heating elements, a SiC heat diffuser was evaluated. Since SiC has a high thermal conductivity of 4.9 W/mK at room temperature and is thermally stable at high temperatures up to 2000°C, it is suitable as a heat diffuser. It has more than four orders of magnitude higher thermal conductivity than any other type of gas. The typical room temperature thermal conductivities of Si and clear fused silica (quartz) is 1.48 and 1.4 W/mK, respectively. By inserting a heat diffuser with high thermal conductivity between the discrete heating elements and the Si wafer, improvement in heat flux uniformity on the Si wafer is expected.

Infrared images of a spiral heater without a heat diffuser and one with a heat diffuser (2-mm-thick SiC disk) are shown in Figs. 4(a) and 4(b). The distance between the heating element and the SiC heat diffuser is maintained at 2 mm. The average heating element temperature is estimated to be ~700°C. A bare spiral heater shows a very large spatial temperature nonuniformity while a spiral heater with a SiC disk (heat diffuser) shows better temperature uniformity at a lower average temperature. Temperature uniformity on the SiC disk can be improved further by increasing the thickness of the SiC disk

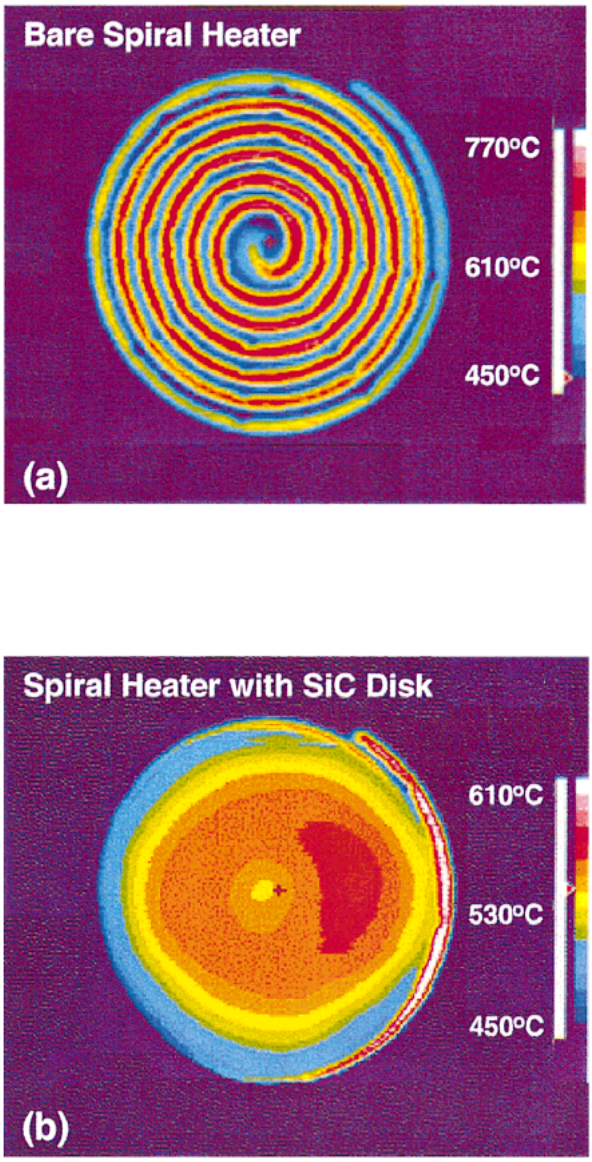

Fig. 4. Infrared image of a spiral heater without heat diffuser (a) and with heat diffuser (2-mm-thick SiC disk) (b).

because a thicker SiC disk diffuses heat more efficiently. A nearly isothermal environment where the wafer is processed can be created by using a combination of discrete heating elements and a SiC heat diffuser.

2.6 Process chamber design

A cross-section of the SWF process chamber is shown in Fig. 5. The process chamber has three standoffs made of quartz and has no moving parts inside. The entire unit (the quartz process chamber, SiC cavity and heater assembly) is enclosed inside an aluminum chamber. The wafers can be processed in either vacuum or atmospheric pressure (1–760 Torr). An R-type (Pt–13% Rh/Pt) thermocouple is embedded in one of the quartz standoffs to monitor the idle process environment temperature and wafer temperature during the process. The wafer is placed on the quartz standoffs (8–9 mm tall) in the middle of the process chamber. The distance between the wafer and quartz walls is maintained at $\sim$10 mm for both upward and downward directions. The quartz process chamber is located in a SiC cavity, which acts as a heat distributor to create an isothermal process environment. The temperature of the SiC cavity is monitored by three embedded R-type thermocouples and controlled by the three-zone heater assembly using feedback signals from the thermocouples to provide an identical and nearly isothermal environment for each wafer regardless of wafer conditions. Two symmetrical edge heaters compensate for the edge heat loss from the heater unit. The process chamber temperature is maintained constant at a predetermined temperature.

2.7 Heat diffuser optimization

The shape effect of heated cavities on within-wafer temperature uniformity was investigated using two different types of SiC cavities. One cavity was configured using two SiC parallel plates (284 mm $\times$ 270 mm $\times$ 5 mm), which were surrounded by a heater assembly. The other cavity was configured with a one-piece SiC tube with a rectangular cavity inside. The distances between the SiC plates in both cavities were maintained constant at 26 mm. A 3-mm-thick quartz

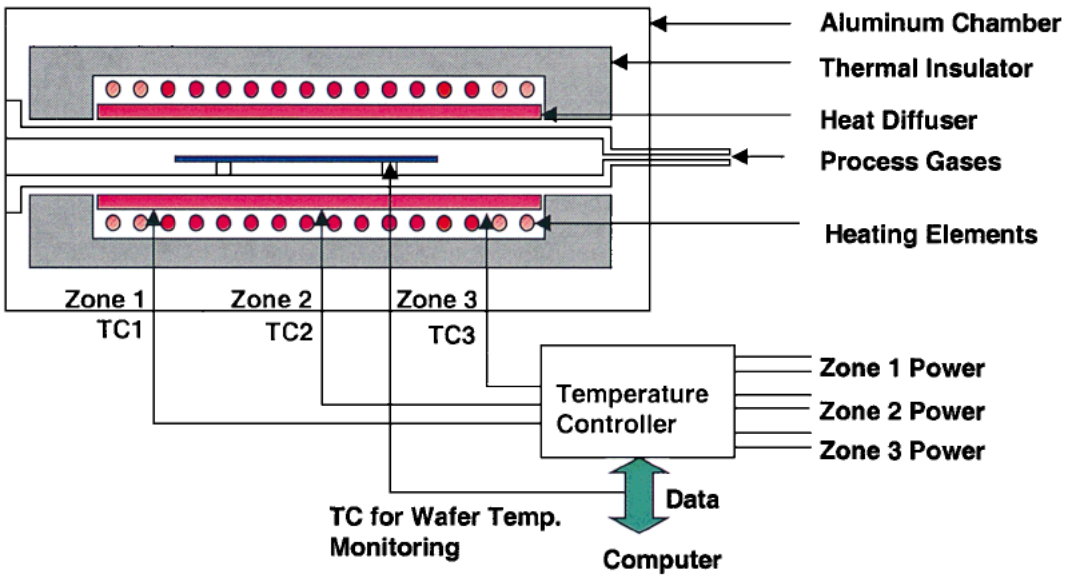

Fig. 5. Cross-section of process chamber including heat source and its temperature controller block diagram.

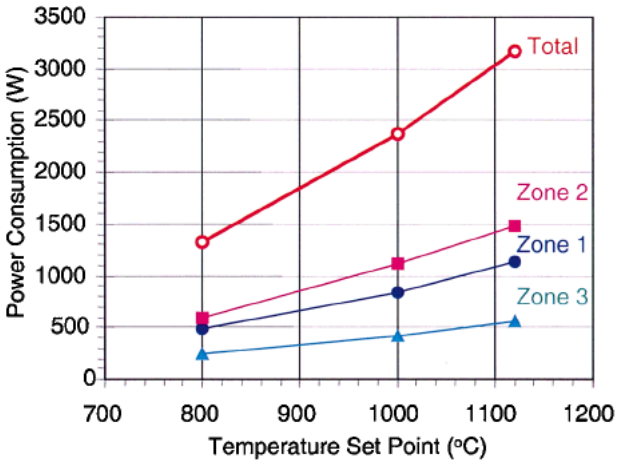

Fig. 6. Power consumption per process chamber as a function of process chamber temperature.

tube was installed between the two SiC parallel plates. This provides a wafer clearances of ~10 mm for both upward and downward directions. The within-wafer temperature uniformity was evaluated in terms of process uniformity as well as crystalline slip generation in the temperature range of 600 to 1150°C.

At temperatures below 800°C, very uniform process results were obtained regardless of the SiC heat diffuser configuration. When two parallel plates are used as a heat diffuser, heat loss from the edge of the parallel plates and the wafer degrades the within-wafer temperature uniformity at temperatures above 800°C. In the case of a one-piece SiC tube cavity, we were able to maintain excellent within-wafer temperature uniformity in the temperature range of 600 to 1150°C by controlling the power of both ends of the SiC cavity. Process uniformity was investigated using the one-piece SiC cavity as a heat diffuser.

2.8 Power consumption

Figure 6 shows the power consumption per process chamber as a function of process chamber temperature. The average steady state power consumption at 1150°C is <3.5 kW per process chamber. Since the SiC cavity temperature is controlled at a steady state, the peak power requirement does not normally exceed twice the average steady state power consumption. Power requirement in a dual chamber SWF system equipped with a vacuum pump is less than 20 kW even at 1150°C operation. In contrast, lamp-based RTP systems consume a peak power of 50 to 250 kW per process chamber at a temperature set point of 1000°C depending on the number of lamps and lamp arrays. The SWF system is very energy efficient and easy to construct without special facility requirements.

3. Wafer Temperature Profile during Process

3.1 Wafer handling sequence

The wafer handling sequence is as follows: (1) the wafer handling robot picks up a wafer, (2) the process chamber gate valve opens, (3) the robot enters and places the wafer into the process chamber, (4) the robot lowers the wafer onto the standoffs, (5) the robot leaves the process chamber, (6) the gate valve closes, (7) the wafer stays in the process chamber for a given process time (8) the gate valve opens, (9) the robot enters into the process chamber, (10) the robot picks up the annealed wafer, (11) the robot removes the wafer from the process chamber at a process temperature, (12) the gate valve closes, (13) the wafer is allowed to cool on the end effector of the robot by radiation and natural convection.

3.2 Wafer temperature profile

The wafer temperature profile during the process at different process chamber (SiC cavity) temperatures is monitored using a thermocouple-embedded instrumentation wafer (Fig. 7). The wafer temperature was measured under 1 atm air environment using a very fine, bare R-type (Pt–13% Rh/Pt) thermocouple bonded on the wafer. The wafer begins to be heated as soon as it is placed into the preheated process chamber. The wafer temperature increases rapidly and approaches the process chamber temperature in less than 20 s. The initial ramp-up rate ranges from 70°C/s to 150°C/s at a process chamber temperature of 1100°C. The wafer is quickly removed after the predetermined processing time at almost the process temperature. An exponential ramp-down is observed during natural cooling. Wafer cooling is normally carried out in a cooling station. The wafer temperature reaches 60°C in less than 60 s from wafer retrieval at 1100°C when cooling is carried out in the cooling station. The idle process environment temperature and wafer temperature during the process can also be monitored using the embedded R-type thermocouple in one of the quartz standoffs.

Typical lamp-heated RTP systems require wafer rotation as well as a dynamic zone temperature control to minimize within-wafer temperature nonuniformity due to pattern transfer from the lamp array during the process. They also require purging and preheating steps before the process, as well as wafer cooling and purging steps after the process. To prevent slip generation during high-temperature processes, a dynamic zone temperature control and slip prevention hardware such as a Si or SiC ring are employed. Rapid ramping up without temperature overshooting has always been a significant technical challenge in designing a lamp-heated RTP system. The process time referred to in a lamp-heated RTP system is the soak time near the process temperature regardless of overhead times such as preheating or ramp-up and ramp-down times.

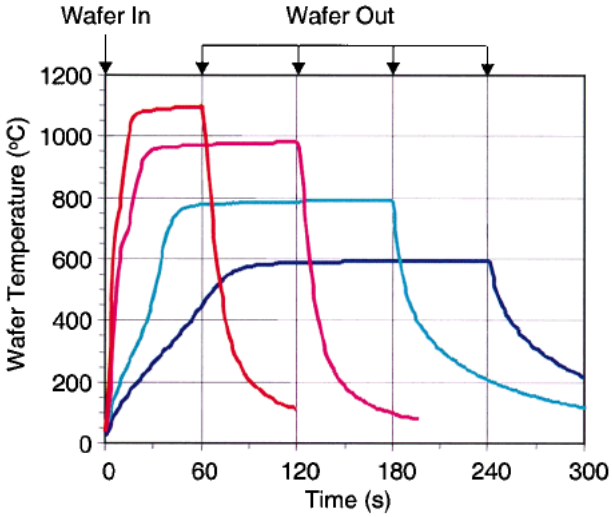

Fig. 7. Wafer temperature profile during processing at different process chamber temperatures.

The overhead time typically ranges from 30 to 120 s.

In a SWF system, temperature overshooting is simply not possible, and excellent temperature repeatability is realized as long as the SiC cavity temperature remains constant. The process time referred to in this paper is the wafer residence time (from wafer-in to wafer-out) in a heated process chamber. The exponential ramp-up and ramp-down rates are considered to be ideal for wafer-friendly and efficient thermal processing without increasing the number of process steps unnecessarily which results in thermal budget increase and productivity decrease.

4. Temperature and Process Uniformity

Within-wafer temperature uniformity was evaluated through process uniformity using process wafers in the temperature range of 600 to 1150°C. Since heat transfer by ambient gas conduction is the predominant wafer heating mechanism at temperatures below 600°C, temperature uniformity within a wafer is strongly dependent on the temperature uniformity of the SiC cavity. Therefore, temperature uniformity evaluation for heating at temperatures below 600°C using process wafers was omitted.

Figures 8(a) and 8(b) show sheet resistance contour maps for 200-mm-diameter wafers before and after TiSi formation. The sheet resistance was measured using a four-point probe; the region 5 mm from the wafer edge was excluded from the measurement. The thickness of Ti films was 80 nm. The annealing condition for TiSi formation was 600°C/60 s and 800°C/60 s. The uniformity change in 1σ after processing the wafers was less than 1.0%, suggesting excellent within-wafer temperature uniformity during the process. Excellent within-wafer temperature uniformity was achieved over the entire silicidation temperature range.

Sheet resistance uniformity of an arsenic implant wafer ($^{75}As^{+}$ 80 keV, $1 \times 10^{16}/cm^2$) after annealing is shown in Fig. 8(c). Annealing was performed at 915°C for 85 s under 760 Torr N_2. The sheet resistance and uniformity were 51.27 Ω/sq. and 0.33% (1σ), respectively.

Thin oxide films were grown on 200-mm-diameter Si wafers. Dry oxidation was performed at 1050°C under 100% O_2 at 760 Torr. The process time was varied from 60 to 3600 s, and the oxygen flowrate of 3 slm was maintained throughout the process. Figure 8(d) shows a thickness-contour map of thin oxide formed in 120 s in the SWF process chamber. Oxide thickness was measured by ellipsometry. An average film thickness of 8.5 nm with uniformity of ∼1.0% in 1σ was obtained.

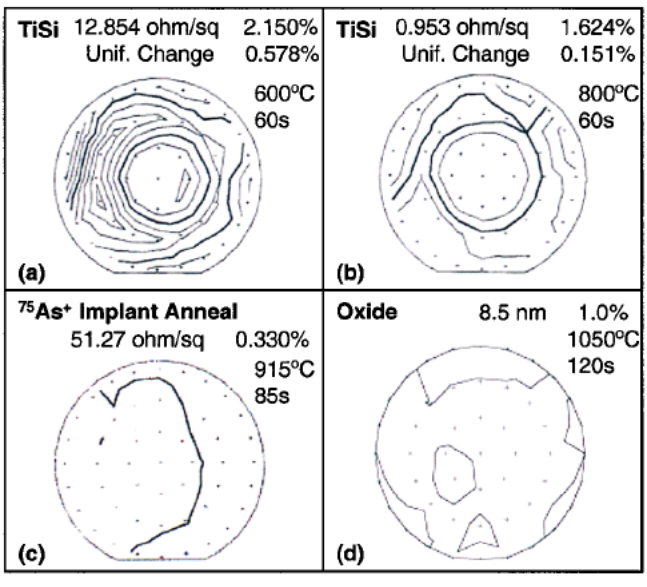

Fig. 8. Sheet resistance and thin film oxide thickness contour maps of wafers processed in SWF.

5. Slip-Free Rapid Thermal Processing

To investigate temperature uniformity and thermal shock during the high-temperature process (>1000°C), bare Si wafers were annealed one to ten times in the temperature range of 800 to 1150°C.

5.1 Process parameter optimization

Si wafers (200-mm-diameter) were annealed in the preheated process chamber in the temperature range of 800 to 1150°C. Crystalline defects generated in the Si wafers during atmospheric pressure annealing were investigated by visual inspection and optical microscopy as a function of temperature, pressure, process time, wafer handling method and speed. A fixed unit process time of 60 s was used. The total process time was varied by repeating the 60 s unit process. Wafers were processed one to five times. Wafers without visible defects were further examined by X-ray topography. The size, shape and spatial distribution of crystal defects generated during RTP were characterized.

Two types of end effector were used in this study. The end effectors were fabricated of clear quartz. One (type A) has three square pads (14 mm × 14 mm in area and 1 mm in height) and the other (type B) has three small rounded dots (∼3 mm in diameter and 1 mm in height). The purpose of using two different types of end effector is to investigate the size and shape effects of contact points. The wafer touches three points (either three square pads or three dots) during wafer transfer to and from the process chamber. The wafer also touches the three quartz standoffs during annealing. The quartz standoffs are at the process chamber temperature.

Figure 9 shows the relative positions of areas in contact with the 200-mm-diameter wafer and schematic illustrations of end effectors A and B. Time lapsed wafer images during natural wafer cooling on the end effectors are also shown. In Fig. 9(a), the three dark areas on the wafer correspond to the three square pads on the end effector. For wafers handled using end effector A with three square pads and processed five times for 60 s each at temperatures above 1050°C, visual slip lines were observed near the contact points along the [100] direction. The length of slip lines is longer when the process temperature is higher. Typical slip lines observed on wafers processed five times at temperatures above 1050°C are shown in Fig. 10. Slip lines were normally observed at the wafer edge and/or area where the wafer made contact with the three square pads on the end effector. When the cold end effector picks up the heated wafer, the contact areas lose heat to the end effector by conduction and radiation. This creates a large temperature gradient near the contact area. Repeated thermal stress in the same area caused formation of crystalline slips. Since the crystalline slips can only occur above a critical temperature, uniform cooling of the wafer from the annealing temperature to the critical temperature is the key to

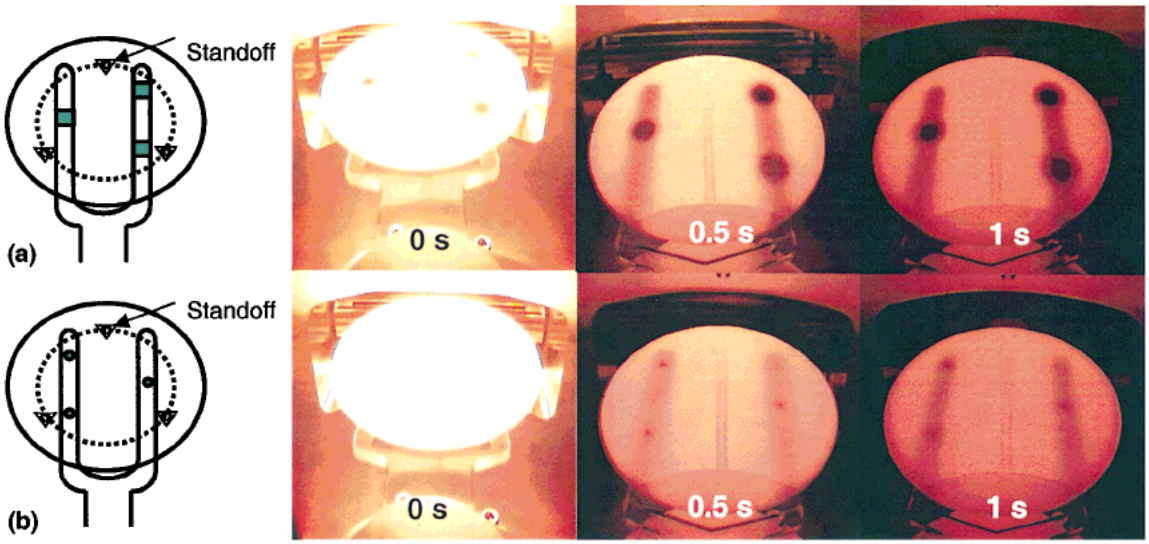

Fig. 9. Time lapsed wafer images during natural wafer cooling on end effector type A (a) and end effector type B (b).

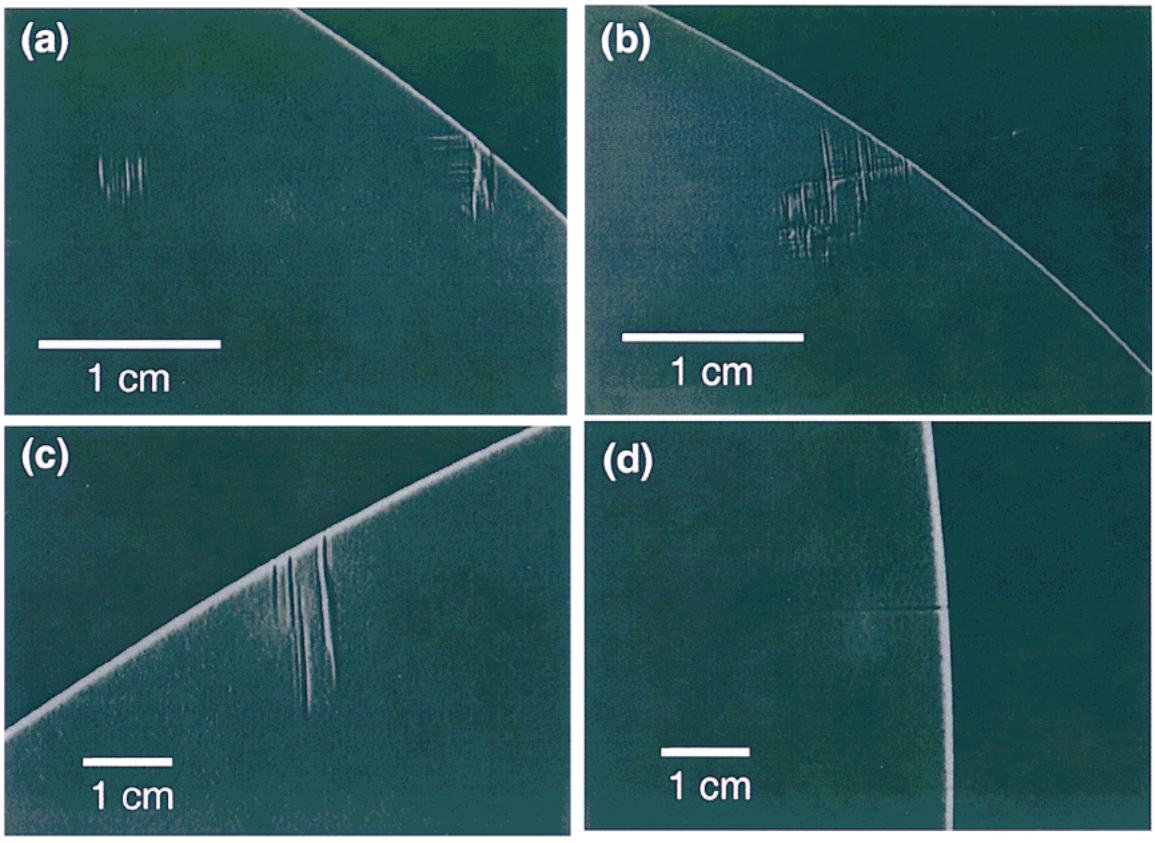

Fig. 10. Typical slip lines observed on wafers processed five times at temperatures above 1050°C under 1 atm air.

preventing crystalline slip formation.

To reduce the thermal stress near the contact area caused by heat loss from the wafer to the end effector, we have designed a new end effector with three small dots (Type B). It reduces the contact area and heat capacity of contact points. In Fig. 9(b), three small dark spots start to appear as time passes. No slip lines were observed in wafers processed five times for 60 s each in the temperature range of 800 to 1150°C by visual inspection and X-ray topography.

5.2 Wafer handling speed

The average wafer transfer (insert and removal) speed was varied between 100 mm/s and 400 mm/s. Wafers transferred slower than 200 mm/s showed some slip lines at temperatures above 1050°C even after a one time annealing for 60 s. Wafers picked up and placed at a speed between 0.5 mm/s and 16 mm/s did not show any difference under visual inspection. All the wafers transferred at a speed faster than 200 mm/s and processed once for 60 s in the temperature range of 800 to 1150°C did not show any slips under visual inspection regard-

less of the pressure and end effector type. Wafers processed five times above 1050°C showed slip lines in areas which came into contact with the end effector. The slip lines become longer as the process temperature and the wafer pick-up speed increase during wafer retrieval after processing. These trends can be explained in that thermal and mechanical stresses increase due to the temperature difference increase between the wafer and the end effector, and the mechanical stress increase on the back surface of the wafer during wafer pick-up. Gravitational stress due to the weight of the 200-mm-diameter Si wafer can cause slip formation above 1200°C if the weight is concentrated in a very small contact area.[5] During the wafer placement in the process chamber, wafers come into contact with standoffs far below the critical temperature for slip generation. Under all process conditions, no slip line was observed at the area where the wafer came into contact with standoffs.

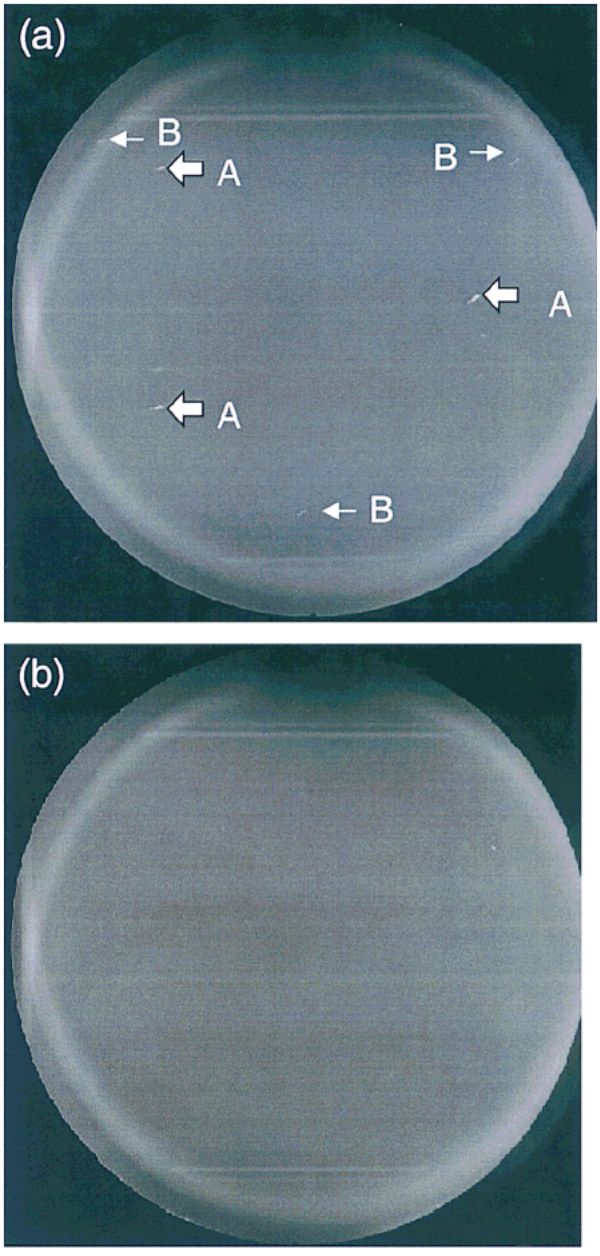

Fig. 11. X-ray topography images of wafers annealed five times at 1100°C for 60 s each under 1 atm air. (wafer pick-up and placement speed: (a) 16 mm/s and (b) 0.5 mm/s).

The effect of wafer pick-up and placement speed was investigated by X-ray topography. Six small white spots corresponding to the three dots (noted by A) on the end effector and contact points (noted by B) with the three standoffs in furnace were observed in the X-ray topography images of all wafers annealed above 1050°C for 60 s. However, the size of the white spots increases as the wafer pick-up and placement speed increases. Figures 11(a) and 11(b) show X-ray topography images of wafers annealed five times at 1100°C for 60 s each with a wafer pick-up and placement speed of 16 and 0.5 mm/s, respectively. In the wafer pick and place speed between 0.5 mm/s and 16 mm/s, no slip lines were observed in wafers annealed five times at 1100°C for 60 s each. This result suggests excellent within-wafer temperature uniformity and excellent gravitational stress management even at high temperatures. The authors believe this rapid RTP technique in the SWF system can be applied to 300-mm-diameter Si wafers by optimizing the process parameters. Details of thermal behavior of 200-mm-diameter Si wafer will be published separately.[11]

6. Conclusions

The design concept of a vacuum- and atmospheric-pressure-compatible, dual chamber SWF system was proposed. The feasibility and production worthiness of a new RTP system were demonstrated with TiSi, As^+ implant annealing and dry oxidation processes. The temperature measurement/control techniques and thermal characteristics of the SWF system were described and compared with those of conventional lamp-heated RTP systems. Uniformity change in sheet resistance before and after the processing was maintained below 1.0% (1σ) in both TiSi processes. The As^+ implantation annealing and dry oxidation results also showed an excellent uniformity of 1.0% (1σ) or less. Due to the dual process chamber configuration and steady-state temperature control, a very high throughput ($\sim$80 wafers per hour for a 60 s process) with minimal power consumption ($<$3.5 kW at 1150°C) was achieved. Thermal behavior and defect generation phenomenon in Si wafers during the RTP process in a SWF system at atmospheric pressure are investigated as a function of temperature, process time, wafer handling method and speed. Size, shape and spatial distribution of crystal defects generated during RTP were characterized using an optical microscope and X-ray topography. The wafer handling method and speed are found to be very important in controlling defect generation during RTP at given process conditions. Highly repeatable slip-free RTP results were achieved in 200-mm-diameter Si wafers processed at 1 atm air, 1100°C (60 s processing up to five times) by optimizing the wafer handling method and speed.

The SWF system is very promising for RTP applications, such as barrier metal annealing, silicidation, oxidation, thin film formation, glass densification, glass reflow, dopant diffusion, thermal donor annihilation and implant annealing up to 1150°C. Many furnace processes can easily be converted to SWF processes without decreasing their productivity. The thermal budget and process cycle time will be reduced significantly. Most RTP processes can also be performed without decreasing the cost performance and/or deteriorating the process results by using the SWF system.

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