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Thermal Behavior of Large-Diameter Silicon Wafers during High-Temperature Rapid Thermal Processing in Single Wafer Furnace

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Thermal behavior of 200-mm- and 300-mm-diameter Si (100) wafers during high-temperature rapid thermal processing (RTP) in a single wafer furnace (SWF) is investigated as a function of temperature, pressure, process time, wafer handling method and speed. Significant elastic wafer shape deformation was observed during wafer temperature ramp-up. Slip generation was frequently observed in wafers processed above 1050°C. Size, shape and spatial distribution of crystal defects generated during RTP were characterized using an optical microscope and X-ray topography. The wafer handling method and speed are found to be very important in reducing defect generation during RTP at the given process conditions. Highly reproducible, slip-free RTP results were achieved in 200-mm- and 300-mm-diameter Si (100) wafers processed at 1100°C by optimizing the wafer handling method and speed. [DOI: 10.1143/JJAP.41.4442]

KEYWORDS: thermal behavior, elastic deformation, defect generation, slip, X-ray topography, single wafer furnace (SWF), rapid thermal processing (RTP)

1. Introduction

In semiconductor thermal processing applications, batch processing was adopted in the early stage in the industry and is still very popular. A typical batch furnace requires a 150–200 wafer load per batch and very long cycle times (from wafer in to wafer out) ranging from 4 to 10 h per batch depending on the process time due to slow ramp-up (~10°C/min) and ramp-down (~3°C/min) rates.[1,2] Batch furnaces are able to meet the requirements for many thermal processing applications, even for 0.18 μm technology.[3]

In addition to the device dimension and allowable thermal budget decrease, the need for improved ambience control due to the introduction of new materials requires a single wafer processing system.[2,3] In terms of thermal budget reduction and process flexibility improvement in operating temperature and lot size, fast ramp mini batch (5–25 wafer load per batch) processing or single wafer rapid thermal processing (RTP) technology has significant advantages over thermal processing in conventional batch furnaces.[1–3] Typical cycle times in the mini batch furnaces and RTP systems are 1–2 h per batch and 1–5 min per wafer, respectively. The ramp-up and ramp-down rate ranges for the mini batch furnaces and the RTP systems are on the order of ~10°C/s and ~100°C/s. Rapid wafer temperature ramp-up and ramp-down make the thermal process very efficient without increasing the thermal budget. However, a small temperature gradient on wafers heated above 1000°C can cause plastic deformation (crystalline slips), which strongly affects device yield.[4,5] Slip-free high-temperature processing of large-diameter (200 mm and above) Si wafers in the fast ramp mini batch furnaces and single wafer RTP systems is difficult.[4,6]

In this study, thermal behavior and defect generation phenomenon in 200-mm- and 300-mm-diameter Si (100) wafers during rapid thermal processing (RTP) in a single wafer furnace (SWF) are investigated as a function of temperature, pressure, process time, wafer handling method and speed. The effects of each of the process parameters are characterized using an optical microscope and X-ray topography. The defect generation mechanism is proposed based on defect characterization results. Wafer handling and process parameters were optimized to establish a slip-free RTP process for 200-mm- and 300-mm-diameter Si wafers.

2. Experiment

Large size (200 mm and 300 mm in diameter) Si (100) wafers were annealed in a preheated SWF process chamber in the temperature range of 800–1150°C. It is well known that the mechanical strength of Si wafers is strongly affected by the impurity type and concentration. The influence of oxygen and boron in Si on the mechanical strength has been studied and published in detail.[7,8] In this experiment, Si wafers with low oxygen concentration were used as control samples. Crystalline defects generated in Si wafers during annealing are investigated by visual inspection and optical microscopy as a function of temperature, pressure, process time, wafer handling method and speed.

For 200-mm-diameter Si wafers, a fixed unit process time of 60 s was used. The total process time was varied by repeating the 60 s unit process. Wafers were processed 1 to 10 times repeatedly to investigate the thermal behavior of Si wafers and the defect generation mechanism. For 300-mm-diameter Si wafers, the unit process time was varied between 60 s and 300 s due to a slower wafer temperature ramp rate compared to that of 200-mm-diameter Si wafers. After thermal processing, visual inspection was performed using the naked eye, an optical microscope and a polarizing infrared microscope. Wafers without visible defects are characterized by X-ray topography. Size, shape and spatial distribution of crystal defects generated during RTP were characterized.

2.1 Experimental apparatus

In the SWF system used in this study, the process chamber is maintained at a predetermined temperature. Wafers are moved in and out of the preheated process chamber instead of the wafer temperature being controlled directly. The SWF process chamber consists of a transparent quartz reactor, a silicon carbide cavity, a heater assembly and an aluminum enclosure. Since the process chamber is made of quartz, the system can be used in oxidation as well as annealing

applications. The process chamber has three standoffs made of quartz and has no moving parts inside. The wafer is placed on the quartz standoffs (8–9 mm tall) in the middle of the process chamber. The distance between the wafer and quartz walls is maintained at ~10 mm for both upward and downward directions. The quartz process chamber is located in a SiC cavity, which acts as a heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The process chamber temperature is kept constant at a predetermined temperature. A nearly isothermal environment in which the wafer is processed is created by the SiC cavity with very high thermal conductivity. The heater assembly is thermally insulated from the outside environment for temperature uniformity and higher energy efficiency. Average steady state power consumption at 1150°C is <3.5 kW per process chamber. Since the SiC cavity temperature is controlled at a steady state, the peak power requirement does not normally exceed twice the average steady state power consumption. In contrast, lamp-based RTP systems consume a peak power of 50–250 kW per process chamber at a temperature set point of 1000°C depending on the number of lamps and lamp arrays. Details of the process chamber are described in the previous report.[9)]

2.2 *Experimental procedure*

Wafers are handled using a clear quartz end effector attached to a three-axis robot. The wafer handling sequence is illustrated in Fig. 1. It is as follows: (1) the wafer handling robot picks up a wafer, (2) the process chamber gate valve opens, (3) the robot enters the wafer into the pre-heated process chamber, (4) the robot places the wafer onto standoffs, (5) the robot leaves the process chamber, (6) the gate valve closes, (7) the wafer is left in the process chamber for a given process time (8) the gate valve opens, (9) the robot enters the process chamber, (10) the robot picks up the processed wafer, (11) the robot removes the wafer from the process chamber at the process temperature, (12) the gate valve closes, (13) the wafer naturally cools on the quartz end effector. During the normal operation of the system, wafers are placed in the cooling station after thermal processing for rapid wafer cooling. It takes ~5 s for the robot to transfer a processed wafer from the process chamber to the cooling station. A wafer unloaded from the process chamber at 1100°C rapidly cools via radiation and convection. For both 200-mm- and 300-mm-diameter Si wafers, the wafer temperature falls far below 900°C in 5 s, which is not the temperature range of concern in this study. Thus, all wafers are cooled on the end effector by natural radiation and convection in this study.

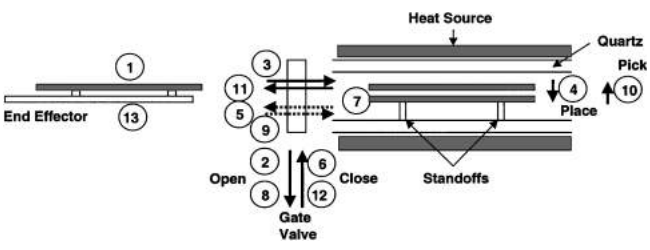


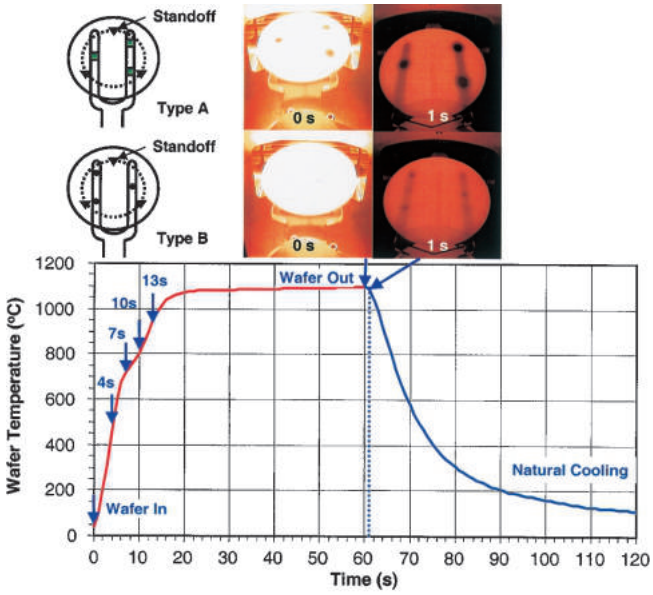
Fig. 1. Illustration of wafer handling sequence.

3. Results and Discussion

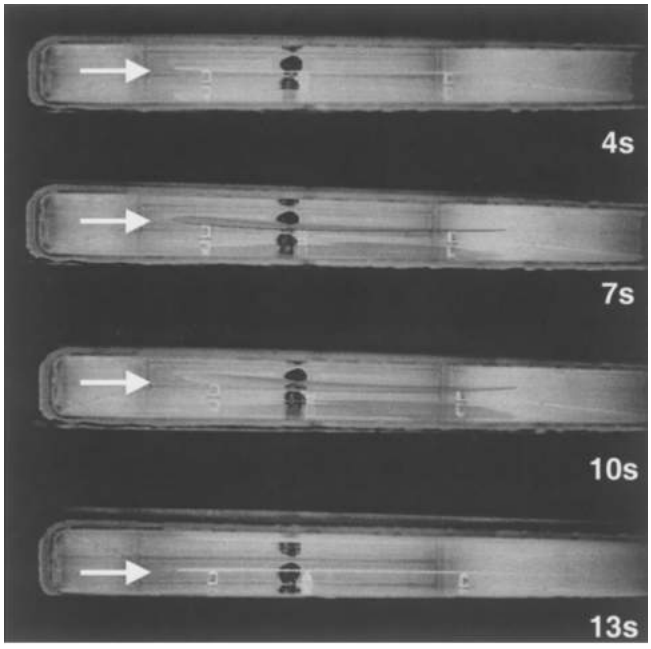
3.1 *Rapid thermal processing of 200-mm-diameter Si wafer*

3.1.1 *Wafer temperature profile*

Figure 2 show the temperature profile of a 200-mm-diameter Si wafer during ramp-up, process and ramp-down along with side-view photographs of the wafer during ramp up and top view photographs of the wafer during wafer removal after annealing. The process chamber temperature



(a)



(b)

Fig. 2. Temperature profile (a) and side view photographs (b) of a 200-mm-diameter Si wafer during annealing (1100°C, 760 Torr air).

and pressure were 1100°C and 760 Torr air, respectively. The wafer temperature was measured using a very fine, bare R-type (Pt–13% Rh/Pt) thermocouple bonded on to the wafer. The wafer is heated as soon as it is placed into the preheated process chamber. The wafer temperature increases rapidly and approaches the process chamber temperature in less than 20 s. The initial ramp rate is ~150°C/s at the process chamber temperature of 1100°C. The wafer is quickly removed after processing at almost the process temperature. An exponential ramp-down is observed during natural cool down. The wafer temperature reaches 60°C in less than 60 s from wafer retrieval at 1100°C when cooling occurs in the cooling station. Since the wafer temperature saturates in 20 s at 1100°C, a unit process time of 60 s was chosen to avoid process-time-related wafer temperature variation.

3.1.2 Elastic deformation during wafer temperature ramp-up

Time elapsed side views of the wafer in the process chamber at 1100°C as seen from the gate valve port during wafer temperature ramp-up are shown in Fig. 2(b). The photographs were taken 4, 7, 10 and 13 s after wafer insertion into the preheated process chamber. The wafer is placed on three quartz standoffs located in the quartz process chamber. The dark hole in the center seen in side-view photographs is the process gas inlet. The wafer shape starts to deform as time passes (wafer temperature increases). A maximum vertical wafer deformation of ~10 mm was observed 10 s from the wafer insertion. An average wafer temperature at 10 s from the wafer insertion is approximately 800°C. The wafer becomes flat at 13 s (~950°C) from the wafer insertion. Temperature nonuniformity within the wafer during rapid wafer temperature ramp up caused the elastic wafer shape deformation due to nonuniform thermal expansion. The wafer temperature becomes uniform in 13 s and the wafer shape becomes flat again.

The higher the process chamber temperature, the more radiation heating becomes the dominant heating mechanism. The edge of the wafer has more surface area per volume than the wafer center, and the radiation heat transfer at the wafer edge is much more efficient. This makes the edge temperature ramp rate faster than that of the wafer center. As a result of this temperature nonuniformity during wafer temperature ramp-up, the wafer deforms significantly. The higher the process chamber temperature becomes, the greater the elastic deformation becomes. The wafer temperature becomes uniform as the wafer temperature saturates near the process chamber temperature due to the thermal conduction within the wafer. As a result, the elastic deformation relaxes with time.

3.1.3 Wafer handling speed

The average wafer transfer (insertion and removal) speed was varied between 100 mm/s and 400 mm/s. Slip lines were observed only on wafers transferred slower than 200 mm/s at temperatures above 1050°C even after a one-time annealing for 60 s. As long as the wafer transfer speed is sufficiently high (>200 mm/s), wafers picked and placed at a speed between 0.5 mm/s and 16 mm/s did not show any slip lines under visual inspection. One time thermal processing in the temperature range of 800–1150°C for 60 s did not add any visually observable crystalline slips on wafers either, regardless of pressure (10–760 Torr) and end effector type. Wafers processed five times at a temperature above 1050°C showed slip lines in the area where the end effector made contact. The shape and size of crystalline slips depends on the contact area between the wafer and end effector. The slip lines become longer as process temperature increases and wafer pick-up speed increases after thermal processing. These trends can be explained as the increase of thermal and mechanical stress due to the increase in the temperature difference between the wafer and the end effector and mechanical stress increase on the wafer back surface during wafer pick-up.

Gravitational stress due to the weight of a 200-mm-diameter Si wafer can cause slips above 1200°C if the weight is concentrated in a very small contact area. A 200-mm-diameter Si wafer with thickness of 0.7 mm weighs approximately 55 g. The density of Si is 2.33 g/cm^3. If the three individual contact areas between the wafer and standoff and/or end effector are in the range of 10–100 μm^2, a large gravitational stress of 5.4–0.54 MPa induced by the weight of the wafer will be applied at individual contact area. Under any process conditions, no slip line was observed in the area where the wafer made contact with standoffs. During the wafer placement in the process chamber, wafers make contact with standoffs far below the critical temperature for slip generation. However, wafer pick-up after thermal processing at elevated temperatures using a cold end effector at a higher speed would make achieving a slip-free process very difficult. A slower wafer pick-up can also be very harmful to slip-free thermal processing because of a large temperature gradient near the contact area with the cold end effector. The conduction heat loss from the wafer to the end effector for an extended period makes slip generation easier. Process parameter optimization in particular during wafer pick-up after thermal processing would be extremely important. The gravitational and thermal stress near the contact area must be minimized to prevent slip generation at an elevated wafer temperature above 1050°C.

3.1.4 Effect of end effector shape during wafer cooling

Two types of end effectors were used for handling 200-mm-diameter Si wafers in this study (Fig. 2). The end effectors were made of clear quartz. One (type A) has three square pads (14 mm × 14 mm in area and 1 mm in height) and the other (type B) has three small rounded dots (~2 mm in diameter and 1 mm in height). The purpose of using two different types of end effector is to investigate the size and shape effect of contact points. The wafer touches three points (either three square pads or three dots) during its transfer to and from the process chamber. The wafer also touches three quartz standoffs during annealing. The quartz standoffs are at process chamber temperature. Time-elapsed wafer images during natural wafer cooling on two different end effectors (type A and B), relative positions of contact area on 200-mm-diameter wafer and schematic illustrations of end effectors are shown in Fig. 2.

When wafers were transported by the end effector A with three square pads and processed five times for 60 s each at

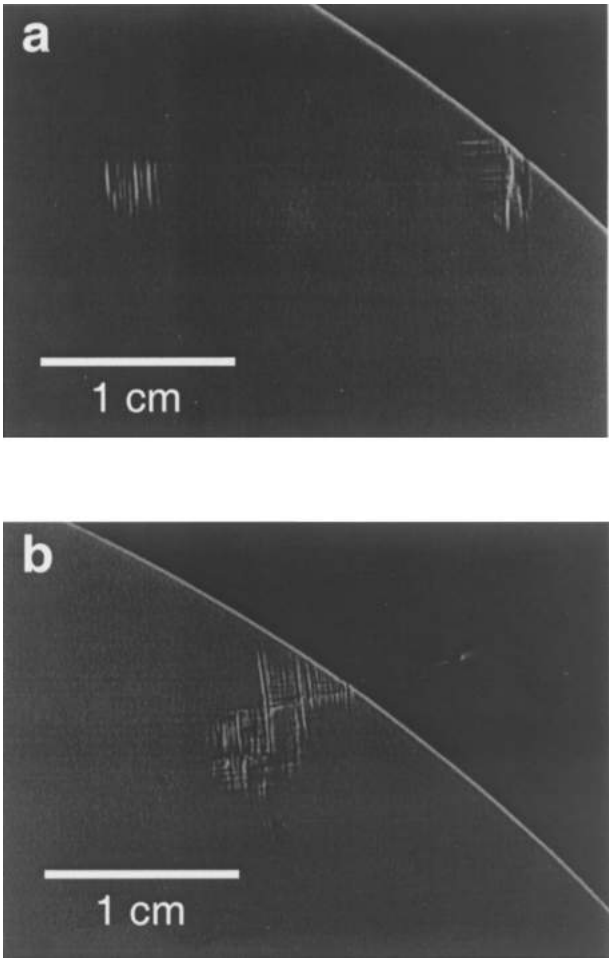


Fig. 3. Optical photographs of typical slip lines observed on 200-mm-diameter Si wafers (1100°C, 60 s, five passes using effector type A).

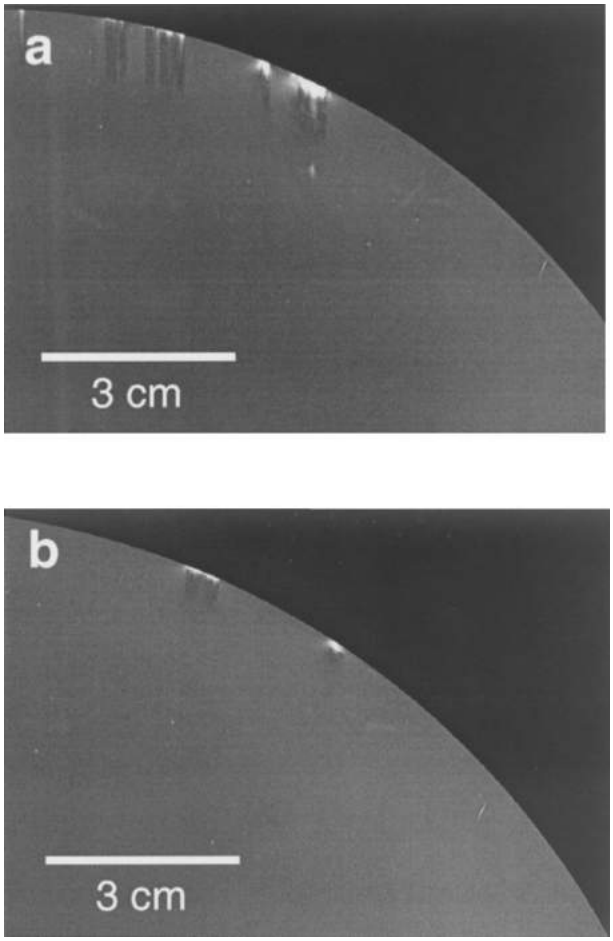


Fig. 4. X-ray topography photographs of typical slip lines observed on 200-mm-diameter wafers removed from the process chamber slowly or for which the heat source is blocked by end effectors for a sufficiently long time (>2 s) (1100°C, 60 s, five passes using effector type B).

temperatures above 1050°C, they showed visual slip lines near the contact points along the [100] direction. The slip lines are longer when the process temperature is higher. Typical slip lines observed on wafers processed five times at temperatures above 1050°C are shown in Figs. 3(a) and 3(b). Slip lines were normally observed at the wafer edge and/or in the area where the wafer made contact with three square pads on the end effector (type A). The three dark areas on the wafer correspond with the three square pads on end effector. When the cold end effector picks up the heated wafer, the contact areas lose heat to the end effector via conduction and radiation. This creates a large temperature gradient near the contact area. Repeated thermal stress in the same area caused crystalline slips.

To reduce the thermal stress near the contact area caused by heat loss from the wafer to the end effector, we have designed a new end effector with three small dots (type B). This is to reduce the contact area and heat capacity of contact points. Time elapsed wafer images during natural wafer cooling on the end effector with three small dots can be seen in Fig. 2. Wafer cooling occured very uniformly. Three small dark spots start to appear as time passes. No slip lines were observed in wafers processed five times for 60 s each in the temperature range of 800–1150°C under visual inspection. In wafers removed from the process chamber slowly or for which the heat source was blocked by end effectors for a sufficiently long time (>2 s), few crystalline slip lines were observed at the robot side edge of the wafers by X-ray topography [Figs. 4(a) and 4(b)].

Figure 5 shows X-ray topography images of wafers annealed five times at 1100°C for 60 s using the end effector with three small dots (type B). The wafer pick-and-place speed was varied between 0.5 mm/s (a) and 16 mm/s (d). Wafer removal at an optimum wafer pick-and-place speed using an end effector with small contact area allows slip-free rapid thermal processing in a pre-heated process chamber environment. Six small white spots corresponding to contact points with three standoffs in the furnace and three dots on the end effector were observed in the X-ray topography image of a wafer annealed five times at 1100°C for 60 s [Figs. 5(c) and 5(d)]. Scratches on the wafer back surface were generally observed by X-ray topography at all supporting points in wafers annealed above 1050°C. This is due to the thermal expansion of Si wafers during high-temperature annealing. No slip lines were observed in wafers annealed five times at 1100°C for 60 s each and handled appropriately. This result suggests that within-wafer temperature uniformity, and thermal and gravitational stress management in SWF were excellent even at high temperatures.

A similar study on thermally induced dislocation in 200-mm-diameter Si wafers has been performed by Karoui *et al.* using a susceptor-based RTP system.[15] The susceptor

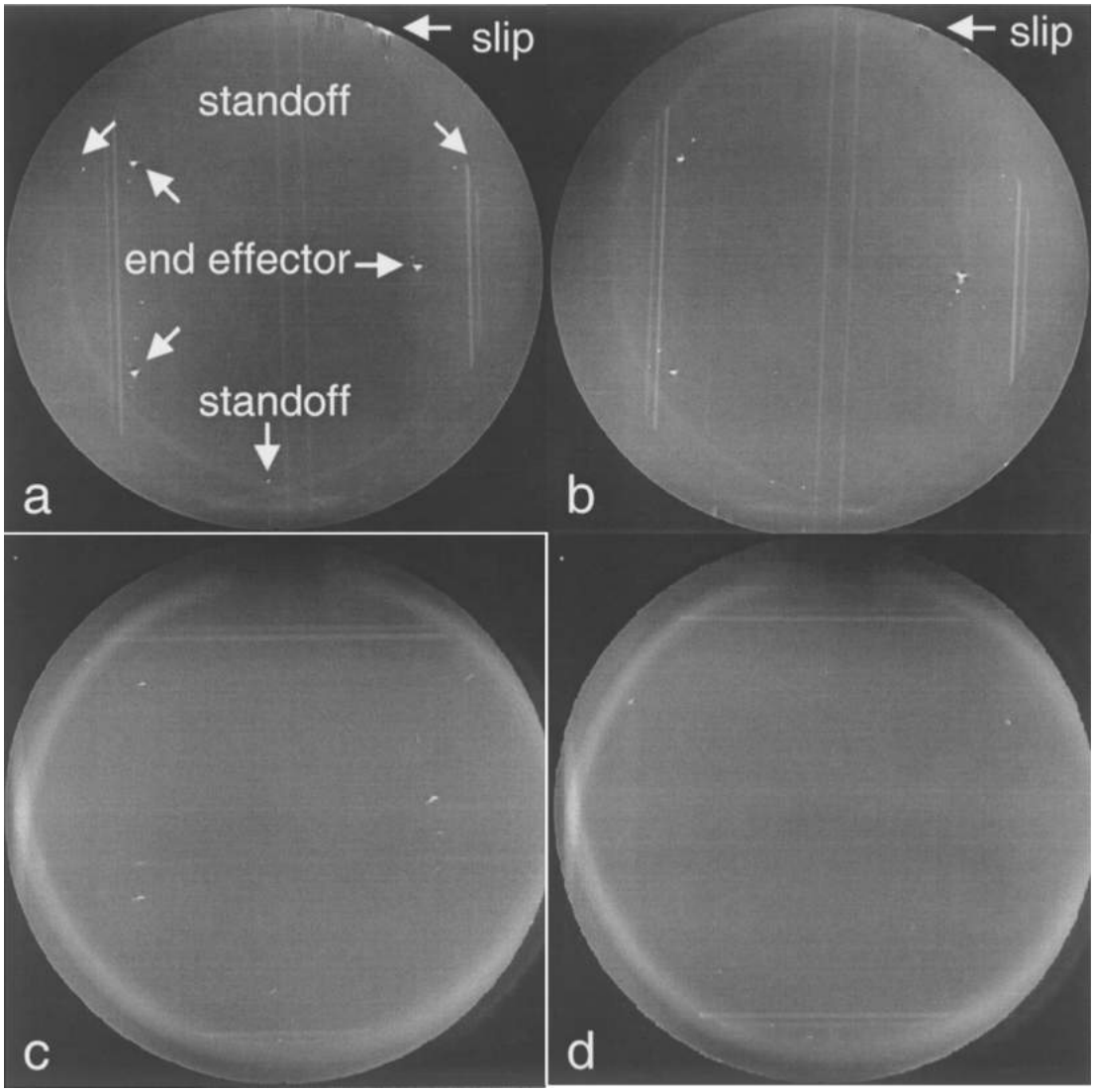


Fig. 5. X-ray topography images of 200-mm-diameter wafers annealed five times at 1100°C for 60 s each using the end effector with three small dots (type B) with different wafer handling speeds (a: 0.5 mm/s, b: 2 mm/s, c: 8 mm/s and d: 16 mm/s).

temperature, wafer lift pin shape, wafer lift speed and wafer preheating time were varied in the study. In the susceptor-based RTP system, two wafers are simultaneously placed side-by-side onto the lift pins, then placed in close proximity to a susceptor by lowering the lift pins. The wafers are heated mainly from the bottom side by the susceptor.[16] After annealing the wafers, the lift pins raise the wafers to wafer pick up position. As the wafers move away from the heated susceptor, the wafer temperature starts to drop prior to the wafer removal from the process chamber. The system operates under a vacuum environment (1–50 Torr). Wafer handling damage in wafers processed above 930°C was observed, but no crystalline slip was observed.[15] The wafer temperature drop prior to the wafer removal from the process chamber and vacuum processing make defect control somewhat easier in the case of annealing using the susceptor-based RTP system.

In the SWF system, a single wafer was heated from both top and bottom in a 1 atm air environment and no lift pins were used for wafer placement in the process chamber. The wafer is directly placed onto and picked up from the quartz standoffs (8–9 mm tall) present in the middle of the process chamber. No wafer cooling from the process temperature is expected prior to the wafer removal from the process chamber since the wafers are heated from both top and bottom. The wafer removal at the process temperature in a 1 atm air environment in the SWF system makes defect prevention difficult.

3.2 Feasibility of slip-free 300-mm-diameter wafer thermal processing

The semiconductor industry has been moving towards larger diameter wafers to reduce the production cost per chip. Large-size Si wafers (300 mm in diameter) became commercially available a few years ago. Unit process development and process integration using 300-mm-diameter wafers are actively being conducted. In thermal processing of 300-mm-diameter wafers, one of the greater challenges is to reduce and eventually eliminate defect generation and subsequent slip generation induced by high-temperature heat treatment. The wafer thickness was increased from 725 μm for a 200-mm-diameter wafer to 775 μm for a 300-mm-diameter wafer. The thickness and diameter increase from 200 mm to 300 mm changes the

Table I. Physical property comparisons between 200-mm- and 300-mm-diameter Si wafers.

	Diameter (mm)	Thickness (μm)	Surface area (cm^2)	Volume (cm^3)	Weight (g)	Surface area/volume (cm^{-1})	Heat capacity (J/K)
Physical	200	725	632.87	22.78	53.07	27.79	37.25
property	300	775	1421.02	54.78	127.64	25.94	89.60
Ratio	1.50	1.07	2.25	2.41	2.41	0.93	2.41

thermal and mechanical behaviors of Si wafers in a heated environment.[5,10] While the thickness increase is only 1.07-fold, the volume and weight increases are 2.41-fold. According to the linear elastic theory for a thin plate, the gravitational bending stress is proportional to r^2/t, where r is wafer radius and t is wafer thickness.[11] When we support 200-mm- and 300-mm-diameter wafers with the same geometrical support structures, the gravitational stress in 300-mm-diameter wafers is more than two times greater than that in 200-mm-diameter wafers. Physical property comparisons between 200-mm- and 300-mm-diameter wafers are summarized in Table I.

Recently, several reports regarding theoretical estimations and experimental results on thermal processing of 300-mm-diameter wafers in conventional furnace and RTP systems have been published.[5,10,11] Nilson and Griffiths[5] have determined the maximum operating temperature by comparing calculated gravitational stresses and temperature-dependent wafer strength. They estimated the allowable stress and allowable temperature variation across the wafer as a function of temperature, wafer size and wafer support geometry. Three support geometries of an edge ring used in a lamp-heated RTP system, inner ring at 70% of the wafer radius and a three-point support at the wafer edge (at angular positions of 0, 90, and 180°) used in batch-type furnaces were considered. The inner ring support showed the maximum allowable temperature as well as the maximum allowable stress.

Fukuda and Hikazutani[10] reported a significant improvement in slip reduction using an inner three-point symmetrical boat in a batch-type vertical furnace. They were able to demonstrate slip free thermal processing up to a temperature of 1000°C using low-oxygen-content wafers and up to a temperature of 1150°C using heavily boron-doped wafers. Their results also indicate that slip lines extend gradually as annealing time increases. In their study, the wafer temperature ramp-up and ramp-down rate above 950°C was kept at 1°C/min. One complete annealing cycle could take 10 h. This is impractical for mass production. On the other hand, Geiler *et al.*[6] reported that thermally induced circularly arranged slip lines and stresses were observed in thermally processed 300-mm-diameter wafers by the scanning infrared depolarization (SIRD) technique. The wafers are processed in a commercially available lamp-based RTP system and the circularly arranged slip lines are speculated to be due to the support ring used in the RTP system.

Since the crystalline slip can only occur above a critical temperature in any given wafer support geometry, the wafer temperature has to be lower than the critical temperature. To reduce thermal stress, temperature variation across the wafer has to be small. The uniform heating of a wafer to the annealing temperature, balanced wafer support during annealing and uniform cooling of the wafer from the annealing temperature to the critical temperature are the keys to preventing crystalline slip formation. According to the literature, the precipitated oxygen level also plays an important role.[5,7,8,12] The maximum allowable temperature difference value for slip-free thermal processing of a 200-mm-diameter Si wafer is reported to be in the range of 2–10°C at 1100°C in the case of wafers with precipitated O_2 concentration of $1 \times 10^{17} \sim 1 \times 10^{18}$ atoms/cm^3, as reported by Leroy and Plougonven.[5,13] The allowable temperature difference value is plotted in Fig. 6 as a function of temperature and O_2 concentration. Figure 7 shows the typical temperature profile of a 200-mm-diameter wafer annealed in the SWF system for 60 s and wafer temperature dependence of allowable temperature difference on the wafer during ramp-up, process and ramp-down based on estimated values using the critical shear stress of Si at different temperatures and O_2 concentrations.[12] Given that Si ingot growth from Si melt is performed at 1420°C, the absolute allowable temperature difference values based on critical shear stress in Si at different temperatures are somewhat questionable. However, the trend of the difference of maximum allowable temperature difference on Si temperature can easily be recognized.

As seen in Figs. 6 and 7, the allowable temperature difference decreases as wafer temperature increases [annealing time increase from wafer insertion (0 s) to wafer removal (60 s) in this case]. Judging from the time elapsed images of a wafer, the within-wafer temperature uniformity around 13 s and beyond from wafer insertion is already better than what is required for the slip-free thermal processing in the SWF system (Fig. 2). Otherwise permanent plastic deforma-

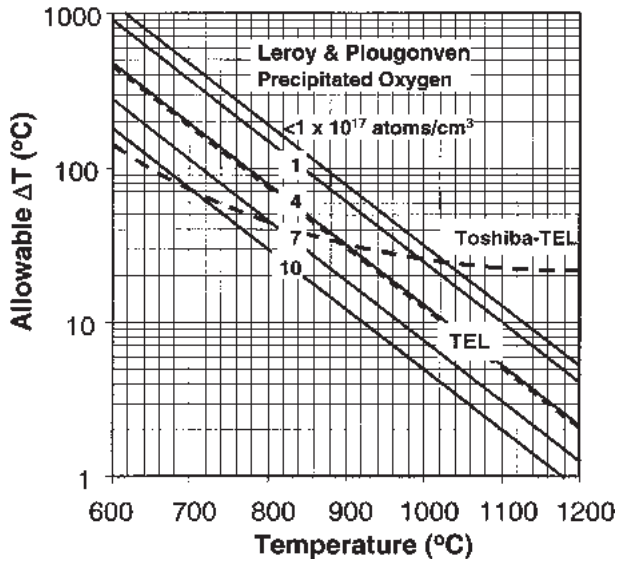


Fig. 6. Allowable temperature difference in 200-mm-diameter Si wafer as a function of wafer temperature and O_2 concentration.[5,13]

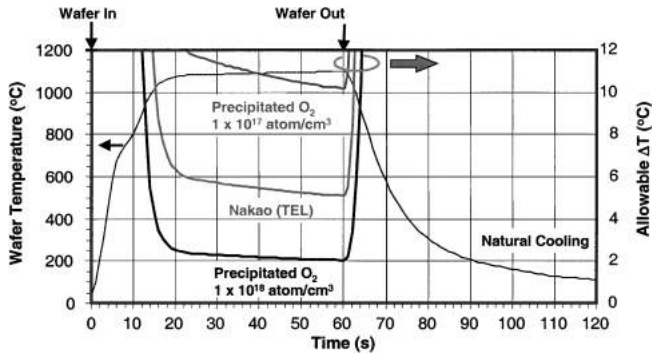


Fig. 7. Temperature profile of a 200-mm-diameter wafer annealed in the SWF system and allowable temperature difference on the wafer during ramp-up, process and ramp-down (1100°C, 60 s, 760 Torr air).

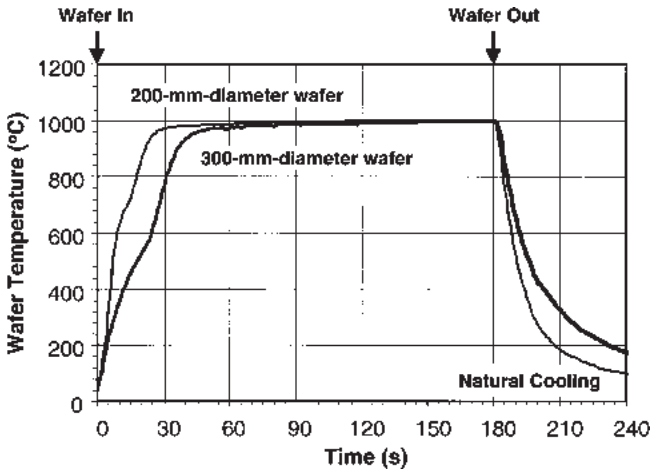


Fig. 8. Temperature profile of 200-mm- and 300-mm-diameter wafers annealed at 1000°C for 180 s under 760 Torr air.

tion will always be seen on wafers processed at 1100°C regardless of the wafer handing method and speed used. During nearly steady state temperature conditions beyond 20 s to wafer removal, the wafer temperature has to be uniform not only to prevent slip generation but also to ensure the process result is uniform. Typical thermal oxidation and implant annealing process results using 49 point measurement show an excellent process uniformity of less than 1% in 1σ.[9,14] Uniform wafer cooling during wafer removal is very critical in preventing crystalline slip generation because the wafer is already very hot and the allowable temperature difference is very small at elevated wafer temperatures. If the wafer temperature falls faster below the critical temperature (~900°C) for slip generation by radiation than for conduction through the contact points on the end effector, one can prevent slip generation during wafer removal from the process chamber.

In the SWF system, wafer temperature uniformity is obtained by maintaining temperature uniformity of nearly isothermal cavity. Thickness increase in 300-mm-diameter wafers helps heat diffusion and improves temperature uniformity during temperature ramp-up. It also reduces elastic deformation during temperature ramp-up. Even though an individual 300-mm-diameter wafer weighs 2.41 times more than a 200-mm-diameter wafer, the combination of the mechanical strength increase by thickness increase and uniform distribution of gravitational stress by inner partial-ring support or three-point support could reduce defect generation in 300-mm-diameter wafers. Given the fact that all the Si wafers were sliced from Si ingots which were grown from Si melt at 1420°C, the authors believe that the slip-free thermal processing of 300-mm-diameter Si wafers up to 1100°C can be performed by this simple RTP technique using the SWF system.

3.3 Rapid thermal processing of 300-mm-diameter Si wafer

Wafer temperature profiles of 200-mm- and 300-mm-diameter Si wafers during annealing at 1000°C for 180 s in the SWF system are plotted in Fig. 8. The 300-mm-diameter wafer was handled using a transparent quartz end effector with minimum contact area. The wafer was placed on the three-point support (quartz standoffs). It took 17.5 s, 21.2 s and 25 s from the time of wafer insertion for a room-temperature, 200-mm-diameter Si wafer to reach 800°C, 900°C and 950°C, respectively. For a 300-mm-diameter Si wafer, it took 31 s, 36 s and 42 s to reach 800°C, 900°C and 950°C, respectively. The 300-mm-diameter Si wafer took 1.7 times longer than the 200-mm-diameter Si wafer to reach 900°C. The 300 mm diameter Si wafer also took longer to cool down than the 200-mm-diameter Si wafer. Considering the heat capacity (volume) increase of 2.41 times in the 300-mm-diameter Si wafer compared to the 200-mm-diameter Si wafer, the wafer heating time of 36 s for the 300-mm-diameter wafer to heat it 900°C is very effective compared to the time of 21.2 s for the 200-mm-diameter Si wafer. Since 300-mm-diameter wafers have a higher heat capacity than 200-mm-diameter wafers, the effect of wafer handling speed on the wafer temperature uniformity is smaller in a 300-mm-diameter Si wafer. The large heat capacity of 300-mm-diameter wafers broadens the wafer handling speed margin compared to that for 200-mm-diameter wafers.

Figure 9 shows an X-ray topography image of a 300-mm-diameter Si wafer annealed at 1050°C for 180 s under

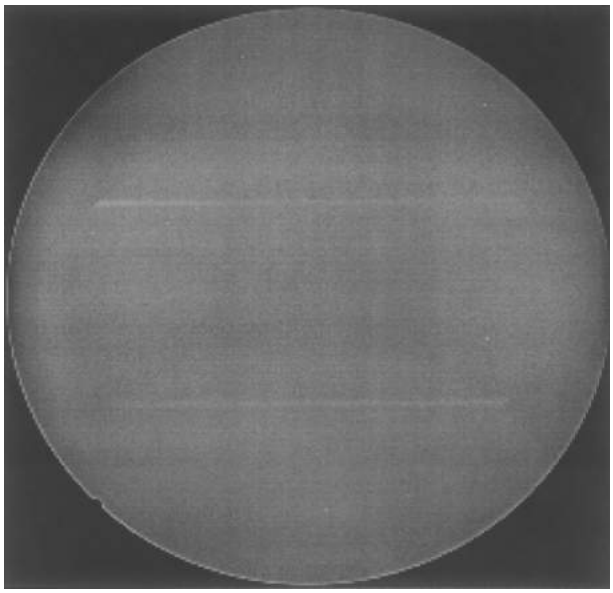


Fig. 9. X-ray topography image of a 300-mm-diameter wafer annealed at 1050°C for 180 s under 760 Torr air.

760 Torr air. No visual slip line was observed in wafers annealed once at 1100°C for 180 s. Small slip lines of up to 3 mm were visually observed in wafers annealed at 1100°C for more than three times under 760 Torr air. The slip line was observed near the stand off area due to the repeated thermal shock and stress. In practice, no wafers will be processed more than once above 1100°C during device fabrication. Power consumption of the process chamber for the 300-mm-diameter Si wafer was slightly less than 3 kW at 1100°C. The energy efficiency of the system is far better than that of lamp-based RTP systems. From this reason, the RTA of 300-mm-diameter Si wafers using the SWF system is very promising as an alternative RTA method.

If severe gravitational and thermal stress management is required, slight wafer cooling prior to wafer pick up would significantly help to preventing slip generation (plastic deformation) in 300-mm-diameter Si wafers. The mechanical strength of wafers increases significantly as wafer temperature decreases. Thermal stress and shock can be greatly reduced by lowering the wafer temperature before picking up the wafer. Wafer cooling prior to the wafer pick up in the process chamber can be realized by introducing a heat shield mechanism in the end effector structure.

4. Summary

The thermal behavior of 200-mm- and 300-mm-diameter Si(100) wafers during high-temperature rapid thermal processing (RTP) in a single wafer furnace (SWF) is investigated as a function of temperature, pressure, process time, wafer handling method and speed. Significant wafer shape deformation was observed during wafer temperature ramp-up. Slip generation was frequently observed in wafers processed above 1050°C when process parameters were not optimized. The size, shape and spatial distribution of crystal defects generated during RTP were characterized using an optical microscope and X-ray topography. The wafer handling method (end effector shape and contact area) and speed are found to be very important in reducing defect generation during RTP at given process conditions. Highly reproducible slip-free RTP results were achieved in 200-mm- and 300-mm-diameter Si(100) wafers processed at 1100°C after optimizing the wafer handling method and speed.

The SWF system is very promising for RTP applications such as: barrier metal annealing, silicidation, oxidation, thin film formation, glass densification, glass reflow, dopant diffusion, thermal donor annihilation and implant annealing up to 1150°C. The feasibility of rapid thermal processing of 300-mm-diameter wafers in the SWF system was discussed based on previous theoretical calculations, experimental results as well as changes in the physical properties of Si wafers from 200 mm to 300 mm in diameter.

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